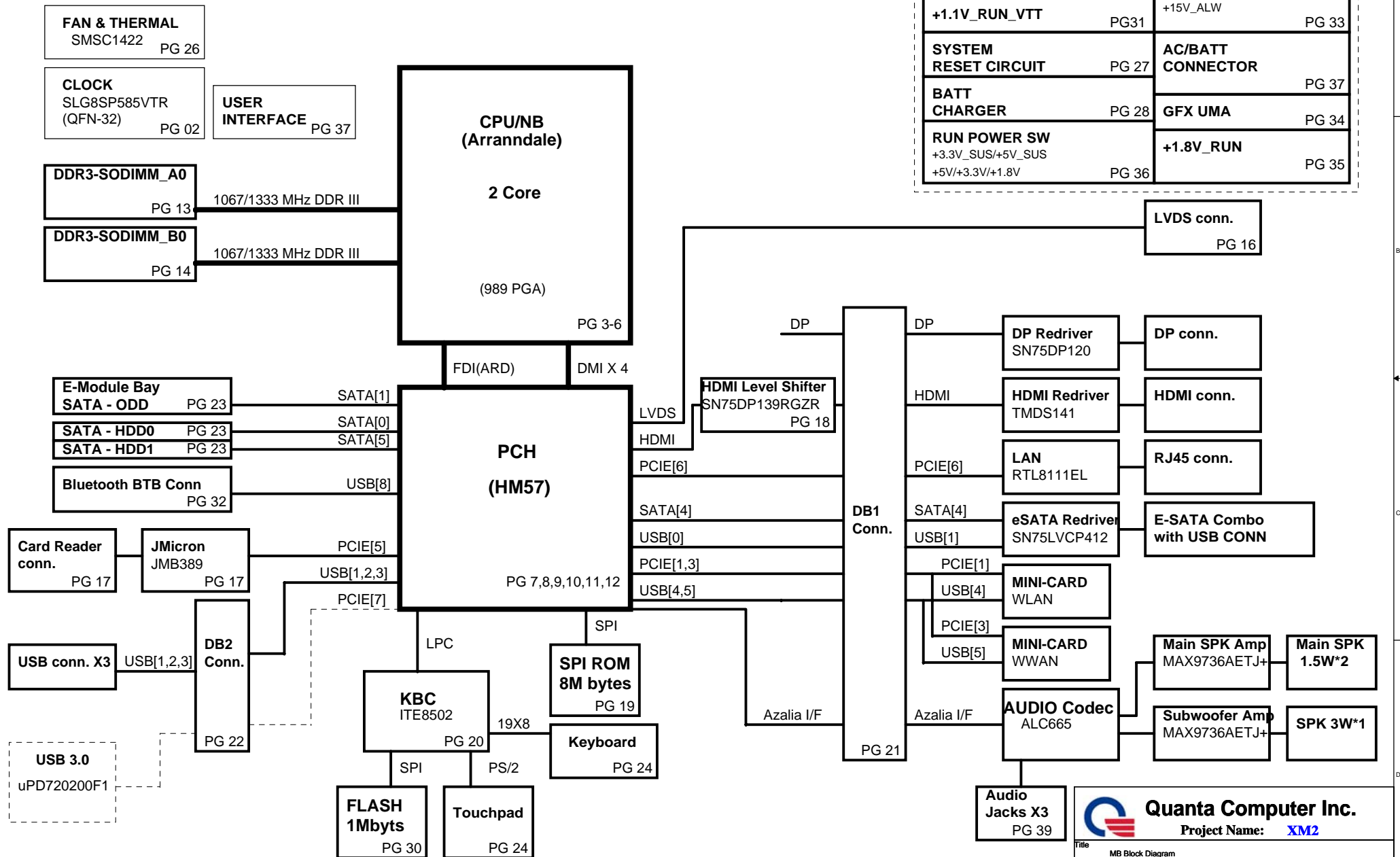
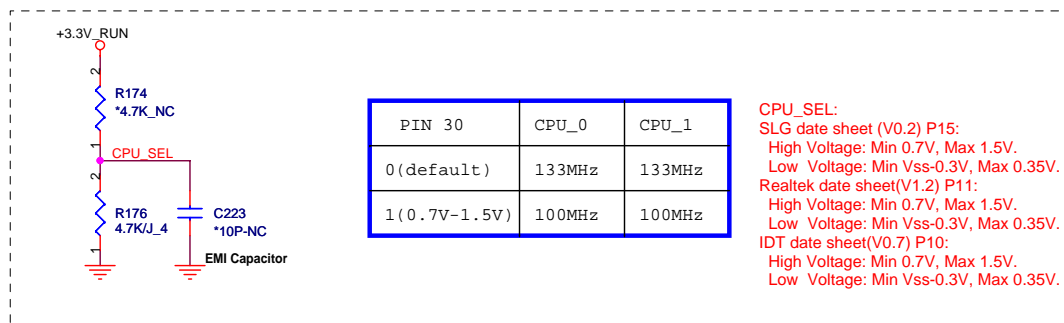
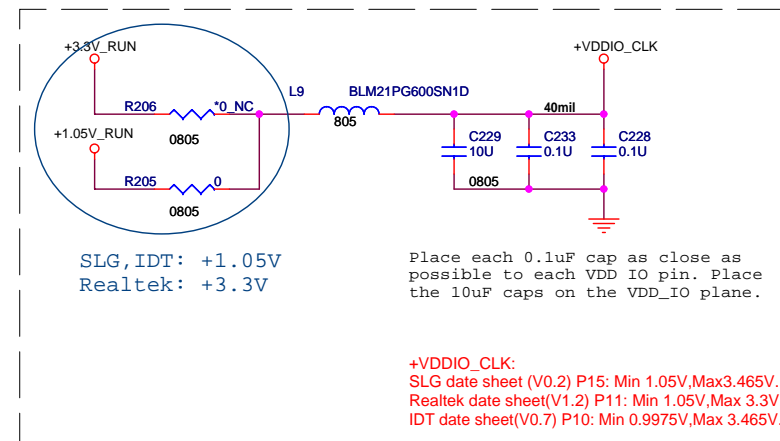
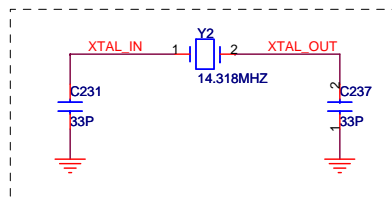
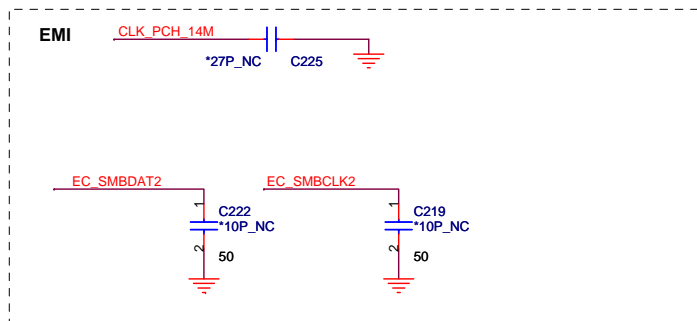
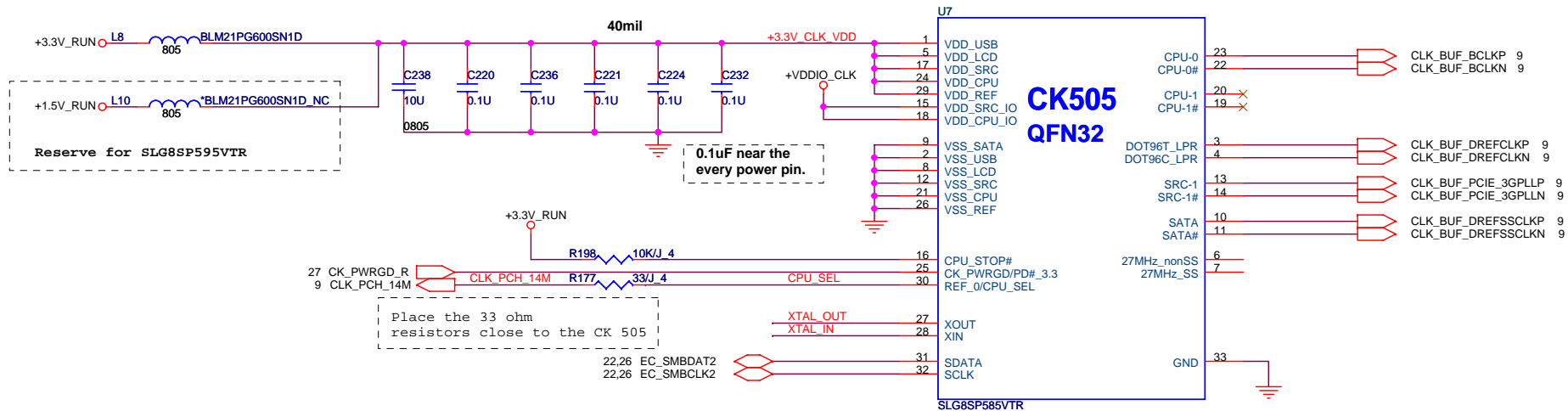


System Block Diagram of GM7

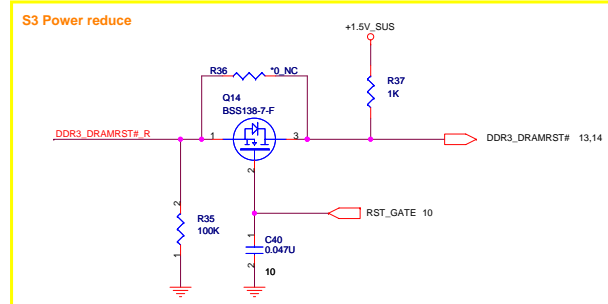
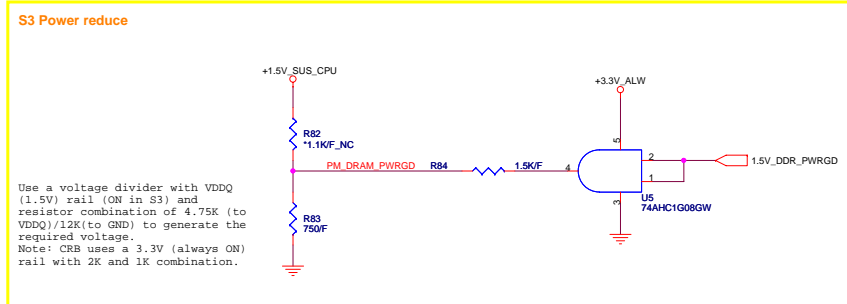
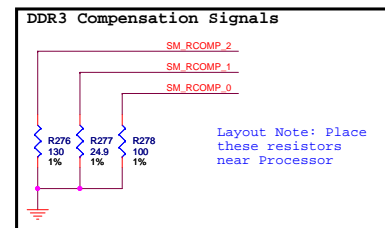
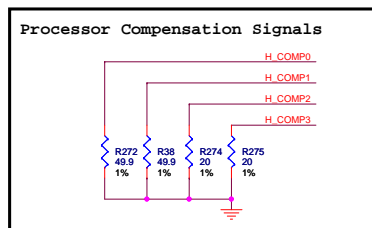
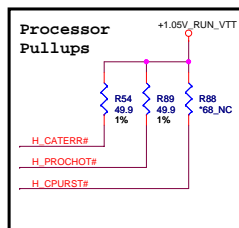
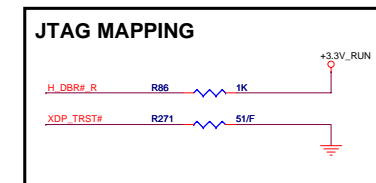
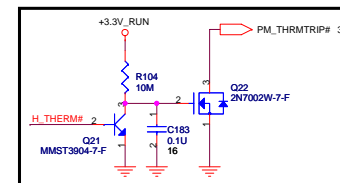
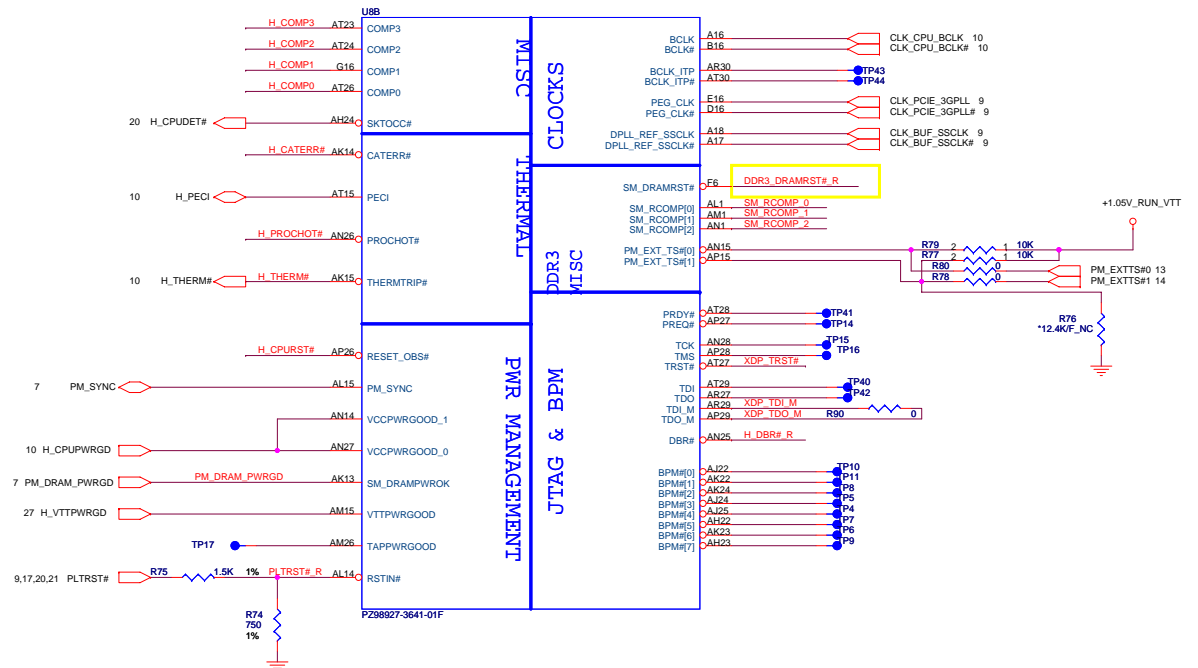


Quanta Computer Inc.
Project Name: **XM2**

Title MB Block Diagram		
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010 Sheet 1 of 40		



AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

UBC

13 M_A_DQ[8:0] M_A_DQ0 A10
M_A_DQ1 C10
M_A_DQ2 A7
M_A_DQ3 A7
M_A_DQ4 B10
M_A_DQ5 D10
M_A_DQ6 E10
M_A_DQ7 A8
M_A_DQ8 DA
M_A_DQ9 E10
M_A_DQ10 E6
M_A_DQ11 E7
M_A_DQ12 E9
M_A_DQ13 B7
M_A_DQ14 E7
M_A_DQ15 C6
M_A_DQ16 H10
M_A_DQ17 DA
M_A_DQ18 K7
M_A_DQ19 J8
M_A_DQ20 G7
M_A_DQ21 G10
M_A_DQ22 J7
M_A_DQ23 J0
M_A_DQ24 L7
M_A_DQ25 M6
M_A_DQ26 M6
M_A_DQ27 L6
M_A_DQ28 L6
M_A_DQ29 K6
M_A_DQ30 N8
M_A_DQ31 P6
M_A_DQ32 A6
M_A_DQ33 A6
M_A_DQ34 A6
M_A_DQ35 A6
M_A_DQ36 A6
M_A_DQ37 A6
M_A_DQ38 A6
M_A_DQ39 A6
M_A_DQ40 A6
M_A_DQ41 A6
M_A_DQ42 A6
M_A_DQ43 A6
M_A_DQ44 A6
M_A_DQ45 A6
M_A_DQ46 A6
M_A_DQ47 A6
M_A_DQ48 A6
M_A_DQ49 A6
M_A_DQ50 A6
M_A_DQ51 A6
M_A_DQ52 A6
M_A_DQ53 A6
M_A_DQ54 A6
M_A_DQ55 A6
M_A_DQ56 A6
M_A_DQ57 A6
M_A_DQ58 A6
M_A_DQ59 A6
M_A_DQ60 A6
M_A_DQ61 A6
M_A_DQ62 A6
M_A_DQ63 A6

13 M_A_BS#0 AC3
13 M_A_BS#1 AB2
13 M_A_BS#2 U7

13 M_A_CAS# AE1C
13 M_A_RAS# AB3C
13 M_A_WE# AE3C

DDR SYSTEM MEMORY - A

SA_CK[0] AA6 M_A_CLK0 13
SA_CK#0 AA7 M_A_CLK0# 13
SA_CKE[0] A7 M_A_CKE0 13

SA_CK[1] Y6 M_A_CLK1 13
SA_CK#1 Y5 M_A_CLK1# 13
SA_CKE[1] P6 M_A_CKE1 13

SA_CS#0 AE2 M_A_CS#0 13
SA_CS#1 AE8 M_A_CS#1 13

SA_ODT[0] AD8 M_A_ODT0 13
SA_ODT[1] AE9 M_A_ODT1 13

SA_DM[0] B9 M_A_DM0 M_A_DM[7:0] 13
SA_DM[1] D7 M_A_DM1
SA_DM[2] H7 M_A_DM2
SA_DM[3] M7 M_A_DM3
SA_DM[4] AG6 M_A_DM4
SA_DM[5] AM7 M_A_DM5
SA_DM[6] AN10 M_A_DM6
SA_DM[7] AN13 M_A_DM7

SA_DQS#0 C9 M_A_DQS#0 M_A_DQS#7[7:0] 13
SA_DQS#1 F9 M_A_DQS#1
SA_DQS#2 J9 M_A_DQS#2
SA_DQS#3 N9 M_A_DQS#3
SA_DQS#4 AH7 M_A_DQS#4
SA_DQS#5 AK9 M_A_DQS#5
SA_DQS#6 AP11 M_A_DQS#6
SA_DQS#7 AT13 M_A_DQS#7

SA_DQS[0] C8 M_A_DQS0 M_A_DQS[7:0] 13
SA_DQS[1] F9 M_A_DQS1
SA_DQS[2] H9 M_A_DQS2
SA_DQS[3] M9 M_A_DQS3
SA_DQS[4] AG8 M_A_DQS4
SA_DQS[5] AM9 M_A_DQS5
SA_DQS[6] AN11 M_A_DQS6
SA_DQS[7] AR13 M_A_DQS7

SA_MA[0] Y3 M_A_A0 M_A_A[15:0] 13
SA_MA[1] W1 M_A_A1
SA_MA[2] AA8 M_A_A2
SA_MA[3] AA3 M_A_A3
SA_MA[4] V1 M_A_A4
SA_MA[5] V8 M_A_A5
SA_MA[6] T1 M_A_A6
SA_MA[7] Y0 M_A_A7
SA_MA[8] Y9 M_A_A8
SA_MA[9] L6 M_A_A9
SA_MA[10] AD4 M_A_A10
SA_MA[11] T2 M_A_A11
SA_MA[12] L3 M_A_A12
SA_MA[13] T3 M_A_A13
SA_MA[14] T3 M_A_A14
SA_MA[15] V9 M_A_A15

14 M_B_BS#0 AB1
14 M_B_BS#1 W5
14 M_B_BS#2 R7

14 M_B_CAS# AC5C
14 M_B_RAS# Y7C
14 M_B_WE# AC6C

UBD

M_B_DQ0 B6
M_B_DQ1 A5
M_B_DQ2 C3
M_B_DQ3 B3
M_B_DQ4 E4
M_B_DQ5 A6
M_B_DQ6 A4
M_B_DQ7 C4
M_B_DQ8 D1
M_B_DQ9 D2
M_B_DQ10 E1
M_B_DQ11 F1
M_B_DQ12 C2
M_B_DQ13 F5
M_B_DQ14 F3
M_B_DQ15 G4
M_B_DQ16 H6
M_B_DQ17 G2
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M_B_DQ56 AN2
M_B_DQ57 AP6
M_B_DQ58 AP6
M_B_DQ59 AT9
M_B_DQ60 AT7
M_B_DQ61 AP9
M_B_DQ62 AR10
M_B_DQ63 AT10

SB_BS[0] AB1
SB_BS[1] W5
SB_BS[2] R7

SB_CAS# AC5C
SB_RAS# Y7C
SB_WE# AC6C

DDR SYSTEM MEMORY - B

SB_CK[0] W6 M_B_CLK0 14
SB_CK#0 W3 M_B_CLK0# 14
SB_CKE[0] M3 M_B_CKE0 14

SB_CK[1] V7 M_B_CLK1 14
SB_CK#1 Y6 M_B_CLK1# 14
SB_CKE[1] M2 M_B_CKE1 14

SB_CS#0 AB8 M_B_CS#0 14
SB_CS#1 AD6 M_B_CS#1 14

SB_ODT[0] AC7 M_B_ODT0 14
SB_ODT[1] AD1 M_B_ODT1 14

SB_DM[0] D4 M_B_DM0 M_B_DM[7:0] 14
SB_DM[1] F1 M_B_DM1
SB_DM[2] H3 M_B_DM2
SB_DM[3] K1 M_B_DM3
SB_DM[4] AL2 M_B_DM4
SB_DM[5] AL2 M_B_DM5
SB_DM[6] AR4 M_B_DM6
SB_DM[7] AR4 M_B_DM7

SB_DQS#0 D5 M_B_DQS#0 M_B_DQS#7[7:0] 14
SB_DQS#1 F4 M_B_DQS#1
SB_DQS#2 J4 M_B_DQS#2
SB_DQS#3 N4 M_B_DQS#3
SB_DQS#4 AH2 M_B_DQS#4
SB_DQS#5 AL4 M_B_DQS#5
SB_DQS#6 AR6 M_B_DQS#6
SB_DQS#7 AR8 M_B_DQS#7

SB_DQS[0] C5 M_B_DQS0 M_B_DQS[7:0] 14
SB_DQS[1] F3 M_B_DQS1
SB_DQS[2] H4 M_B_DQS2
SB_DQS[3] M5 M_B_DQS3
SB_DQS[4] AG2 M_B_DQS4
SB_DQS[5] AL5 M_B_DQS5
SB_DQS[6] AP5 M_B_DQS6
SB_DQS[7] AR7 M_B_DQS7

SB_MA[0] U5 M_B_A0 M_B_A[15:0] 14
SB_MA[1] V2 M_B_A1
SB_MA[2] V3 M_B_A2
SB_MA[3] V3 M_B_A3
SB_MA[4] R1 M_B_A4
SB_MA[5] R2 M_B_A5
SB_MA[6] R6 M_B_A6
SB_MA[7] R6 M_B_A7
SB_MA[8] R4 M_B_A8
SB_MA[9] R5 M_B_A9
SB_MA[10] AB5 M_B_A10
SB_MA[11] P3 M_B_A11
SB_MA[12] R3 M_B_A12
SB_MA[13] AF7 M_B_A13
SB_MA[14] P5 M_B_A14
SB_MA[15] N1 M_B_A15

P298927-3641-01F

P298927-3641-01F

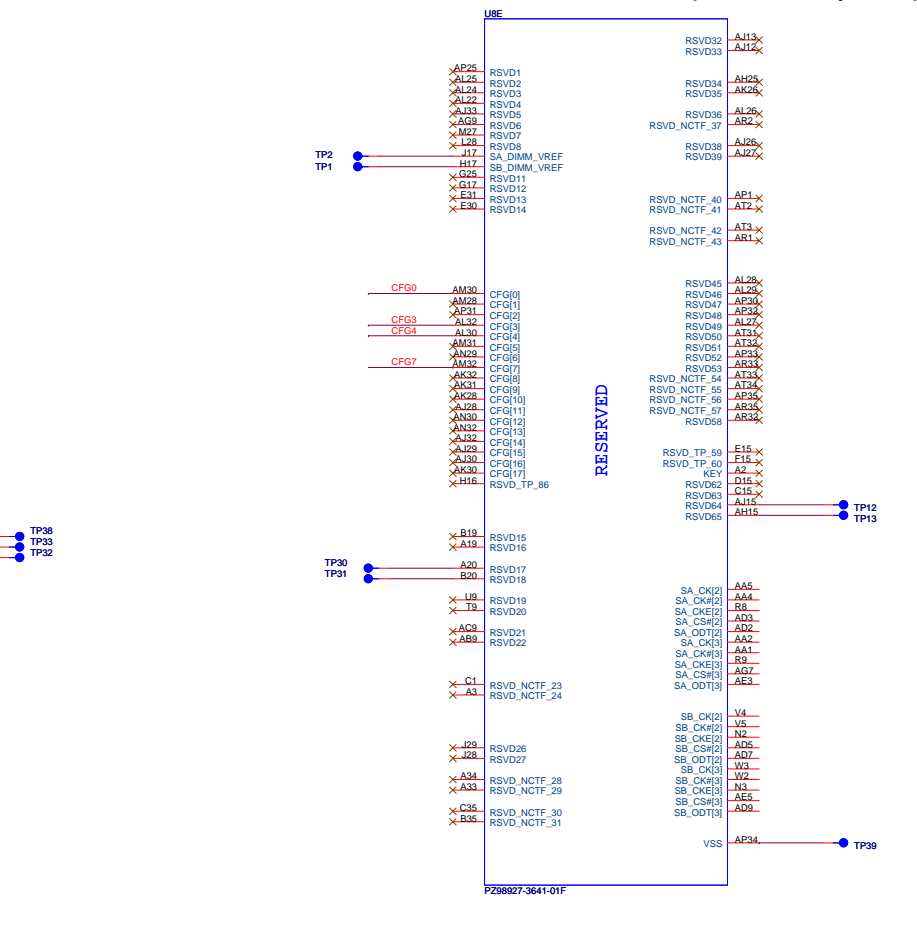
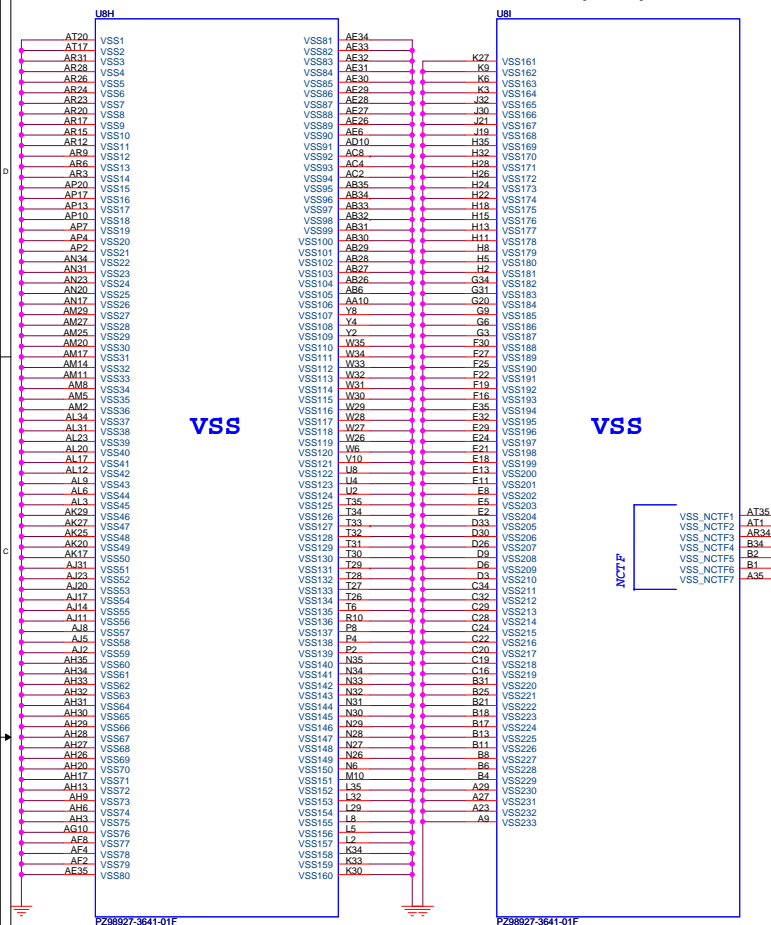


Quanta Computer Inc.
Project Name: XM2

File	CPU 24(DDR)	Rev	D
Size	Document Number XM2_MB		
Date: Friday, January 15, 2010	Sheet 4 of 40		

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)

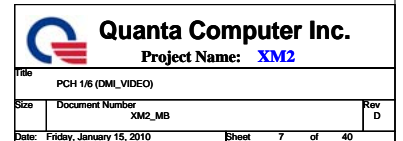


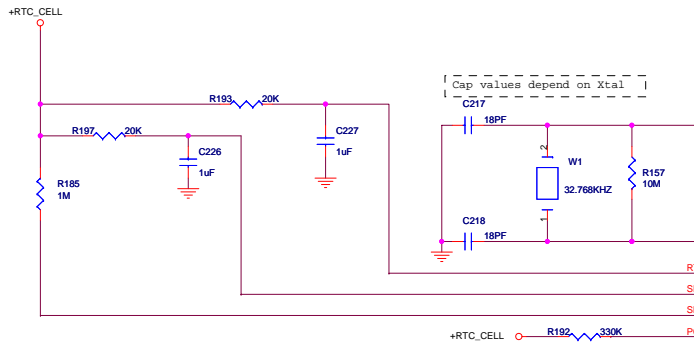
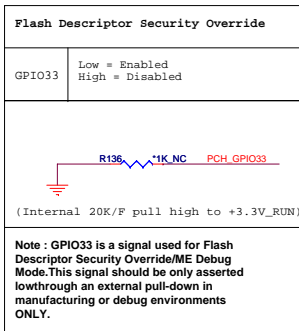
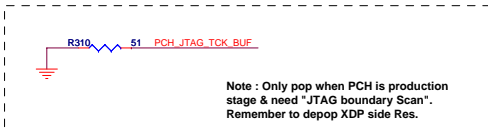
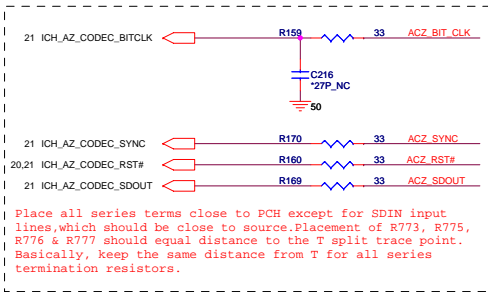
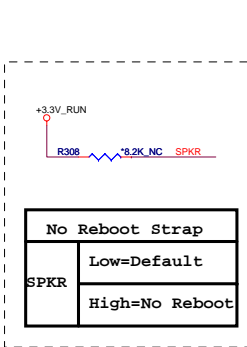
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



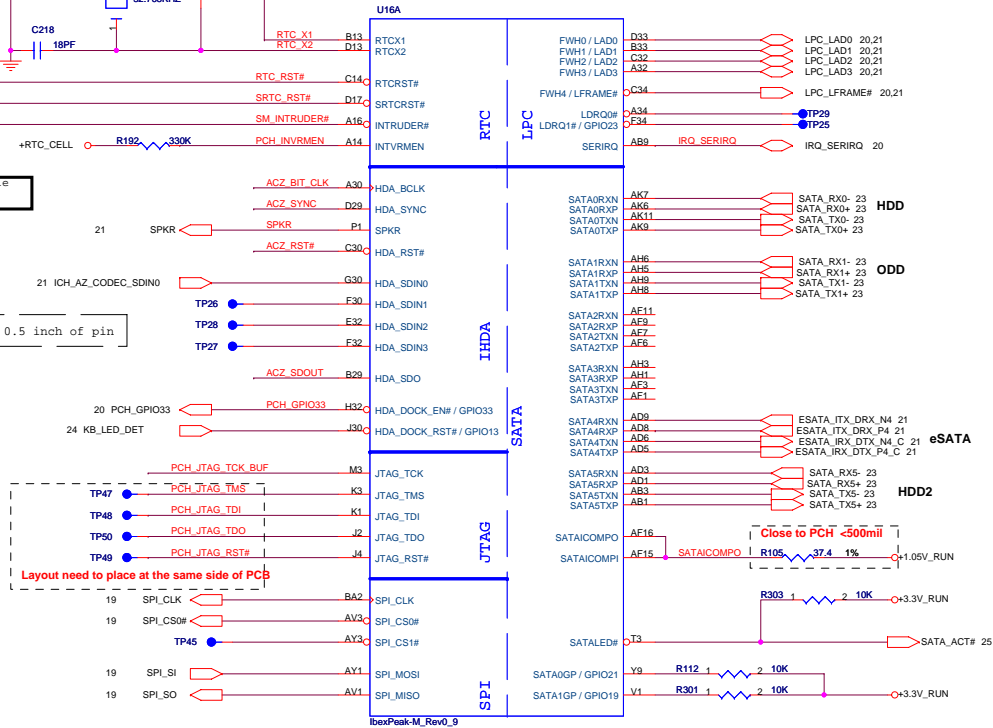
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed
CFG7 Clarksfield (only for early samples pre-ES1)	Common motherboard design	For early samples pre-ES1 CFD

IBEX PEAK-M (LVDS, DDI)



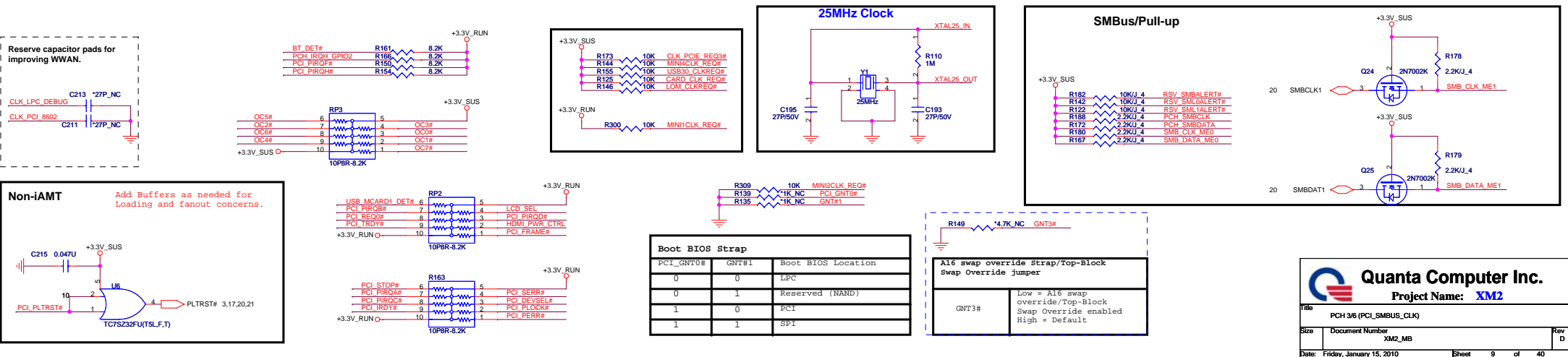
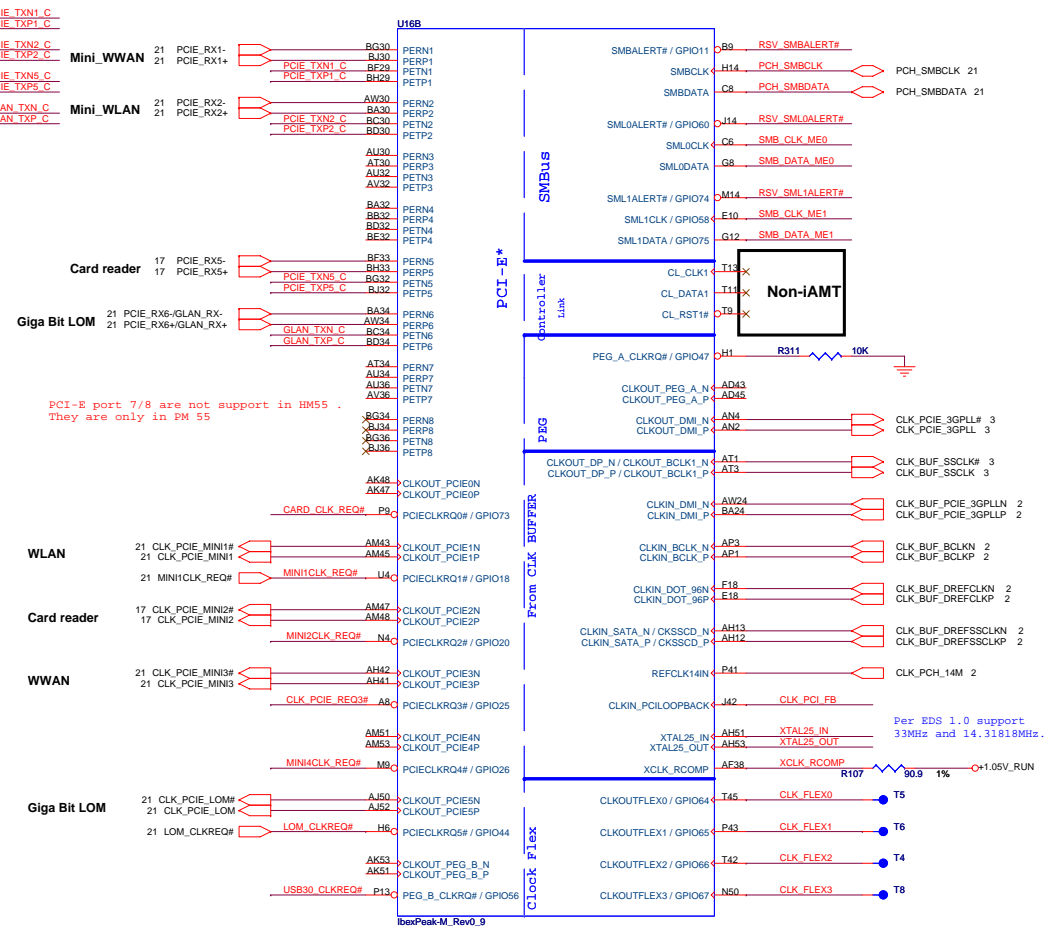
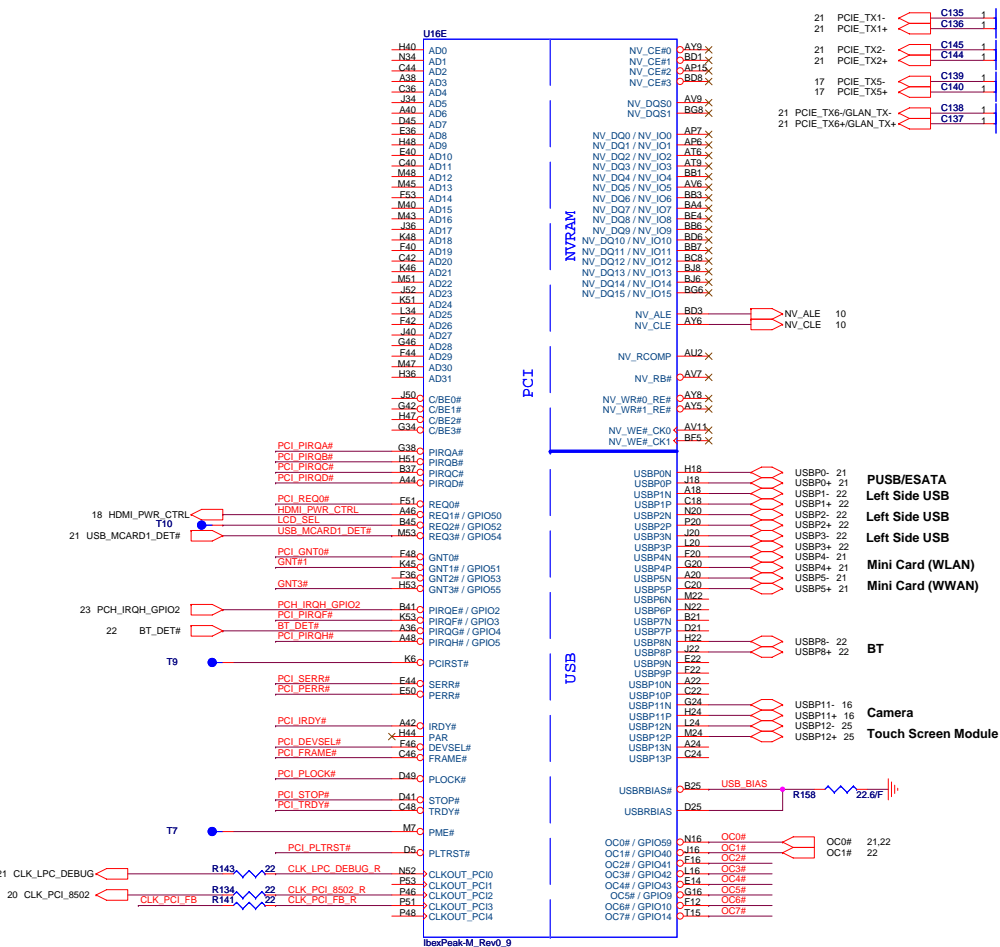


IBEX PEAK-M (HDA,JTAG,SATA)



IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)



[illegible]

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

GPIO Pull-up/Pull-down

S3 Power reduce

Integrated Clock Chip Enable

DMI Termination Voltage

Danbury Technology Enabled

Quanta Computer Inc.
Project Name: **XM2**

File: PCH 4/6 (GPIO)
Size: Document Number XM2_MB
Date: Friday, January 15, 2010 Sheet 10 of 40

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

U16F

MISC

- BMBUSY# / GPIO0 Y3C
- SIO_EXT_SMI# C38
- SIO_EXT_SC# D37
- SIO_EXT_WAKE# J32
- RSV_GPIO8 F10
- LAN_DISABLE# K9
- CR_WAKE# T7
- dGPU_HOLD_RST# AA2
- GPIO17 F38
- PCIE_MCARD2_DET# Y7
- PCIE_MCARD1_DET# R H10
- GPIO27 AB12
- TP_PCH_GPIO28 V13
- USB_MCARD2_DET# M11
- GPIO35 VB
- dGPU_PWR_EN# AB7
- dGPU_PRSTNT# AB13
- WLAN_RADIO_DIS# V3
- BT_RADIO_DIS# P3
- RST_GATE E1
- WWAN_RADIO_DIS# AB6
- CPPE_N# AA4
- GPIO57 F8

CPU

- CLKOUT_BCLK0_N / CLKOUT_PCIEB N
- CLKOUT_BCLK0_P / CLKOUT_PCIEB P
- SCLOCK / GPIO22
- MEM_LED / GPIO24
- GPIO27
- GPIO28
- STP_PCIN# / GPIO34
- SATACLKREQ# / GPIO35
- SATA2GP / GPIO36
- SATA3GP / GPIO37
- SLOAD / GPIO38
- SDATAOUT0 / GPIO39
- PCIECLKRQ6# / GPIO45
- PCIECLKRQ7# / GPIO46
- SDATAOUT1 / GPIO48
- SATA5GP / GPIO49
- GPIO57

NCTF

- VSS_NCTF_1 X A4
- VSS_NCTF_2 X A49
- VSS_NCTF_3 X A5
- VSS_NCTF_4 X A50
- VSS_NCTF_5 X A51
- VSS_NCTF_6 X A52
- VSS_NCTF_7 X B4
- VSS_NCTF_8 X B2
- VSS_NCTF_9 X B3
- VSS_NCTF_10 X BE1
- VSS_NCTF_11 X BF1
- VSS_NCTF_12 X BF3
- VSS_NCTF_13 X BH1
- VSS_NCTF_14 X BH2
- VSS_NCTF_15 X BH3
- VSS_NCTF_16 X BJ1
- VSS_NCTF_17 X BJ2
- VSS_NCTF_18 X BJ4
- VSS_NCTF_19 X BJ5
- VSS_NCTF_20 X BJ6
- VSS_NCTF_21 X BJ7
- VSS_NCTF_22 X BJ8
- VSS_NCTF_23 X BJ9
- VSS_NCTF_24 X BJ10
- VSS_NCTF_25 X BJ11
- VSS_NCTF_26 X BJ12
- VSS_NCTF_27 X D1
- VSS_NCTF_28 X D2
- VSS_NCTF_29 X D3
- VSS_NCTF_30 X E1
- VSS_NCTF_31 X E3

GPIO

- AH45 TP21
- AH46 TP18
- AF48 TP20
- AF47 TP19
- U2 SIO_A20GATE
- AM3 CLK_CPU_BCLK# 3
- AM1 CLK_CPU_BCLK 3
- BG10 H_PECI 3
- T1 SIO_RCIN#
- BE10 SIO_RCIN# 20
- BD10 H_CPUPWRGD 3
- BA22 TP1
- AW22 TP2
- BB22 TP3
- AY45 TP4
- AY46 TP5
- AV43 TP6
- AV45 TP7
- AF13 TP8
- M18 TP9
- N18 TP10
- AJ24 TP11
- AK41 TP12
- AK42 TP13
- M32 TP14
- N32 TP15
- M30 TP16
- N30 TP17
- H12 TP18
- AA23 TP19
- AB45 NC_1
- AB38 NC_2
- AB42 NC_3
- AB41 NC_4
- T39 NC_5
- P6 INIT3_3V#
- C10 TP24

RSVD

GPIO Pull-up/Pull-down

- CR_WAKE# R121 1K
- TP_PCH_GPIO28 R118 10K
- GPIO45 R312 10K
- RST_GATE R313 10K
- GPIO57 R164 10K
- LAN_DISABLE# R156 10K
- RSV_GPIO8 R153 10K
- CPPE_N# R294 10K
- PCIE_MCARD2_DET# R114 10K
- PCIE_MCARD1_DET# R171 10K
- SIO_EXT_SMI# R162 10K
- SIO_EXT_SC# R165 10K
- SIO_EXT_WAKE# R132 10K
- dGPU_PWR_EN# R106 10K
- GPIO17 R138 10K
- SIO_RCIN# R302 10K
- SIO_A20GATE R299 10K
- dGPU_HOLD_RST# R295 10K
- dGPU_PRSTNT# R113 10K
- BT_RADIO_DIS# R308 10K
- USB_MCARD2_DET# R147 10K
- WLAN_RADIO_DIS# R296 10K
- BMBUSY# R297 10K
- WWAN_RADIO_DIS# R111 10K

Integrated Clock Chip Enable

(Reserve to validate for future platforms)

RSV_GPIO8 Enable when sampled low
Disable when sampled high

DMI Termination Voltage

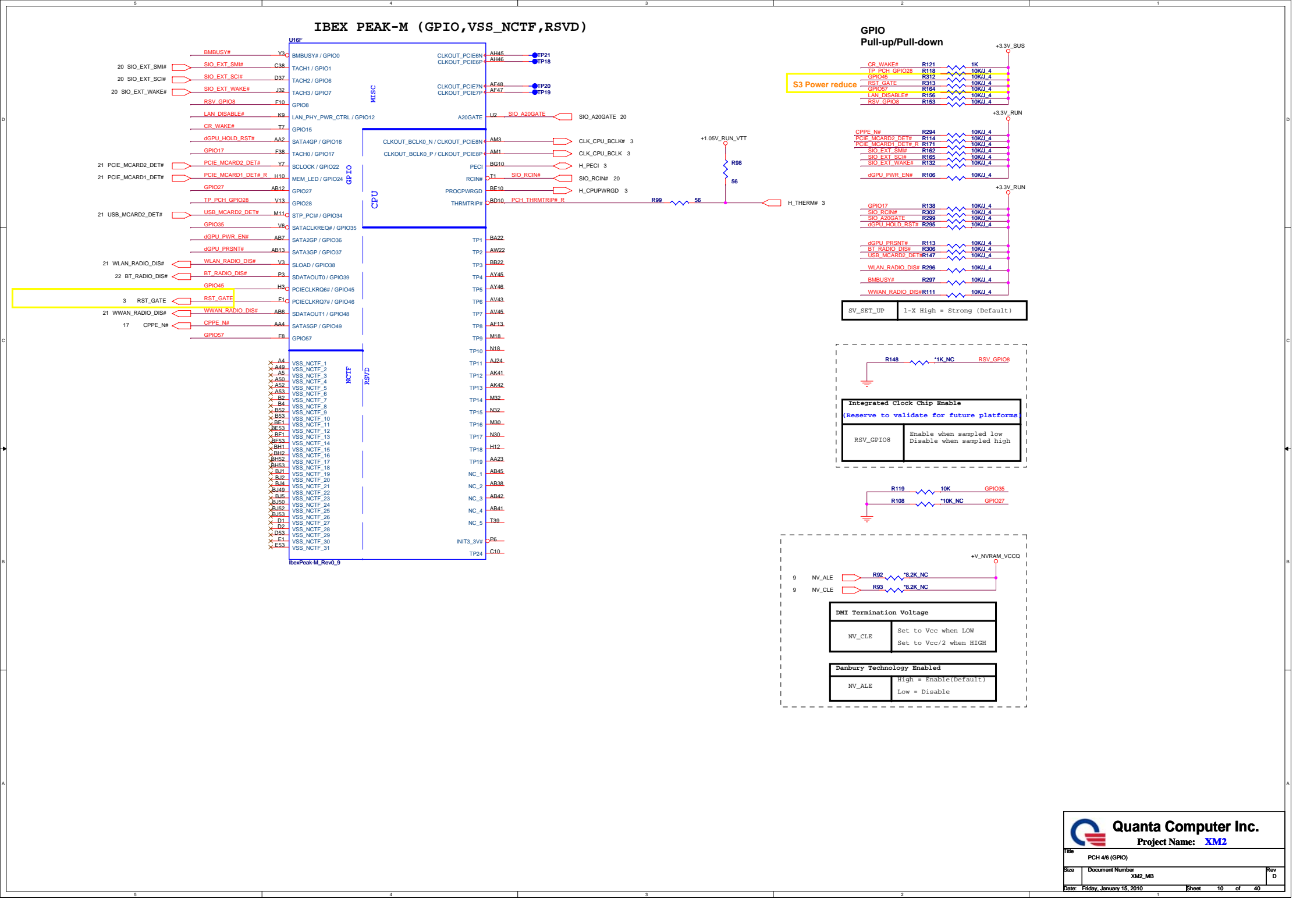
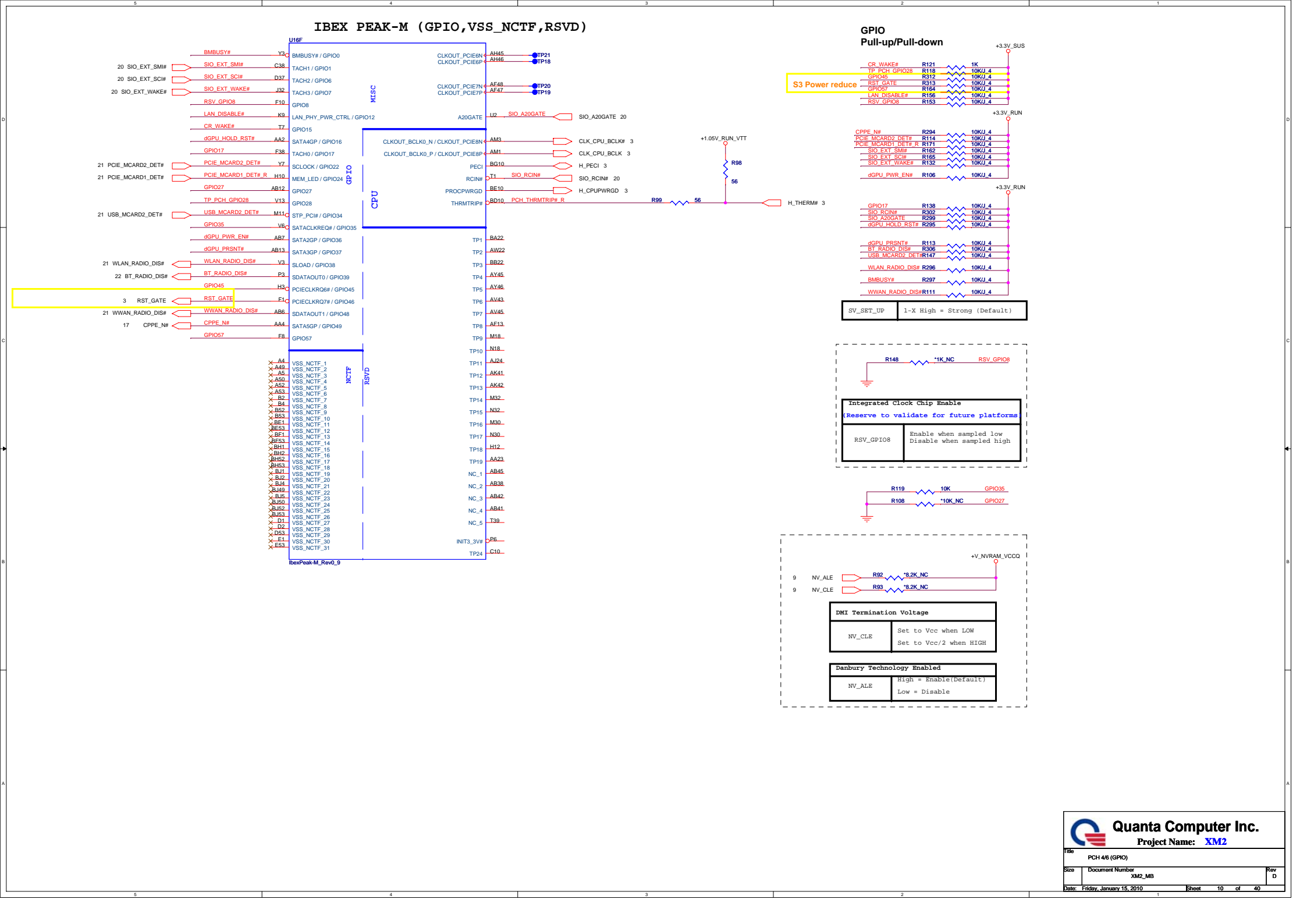
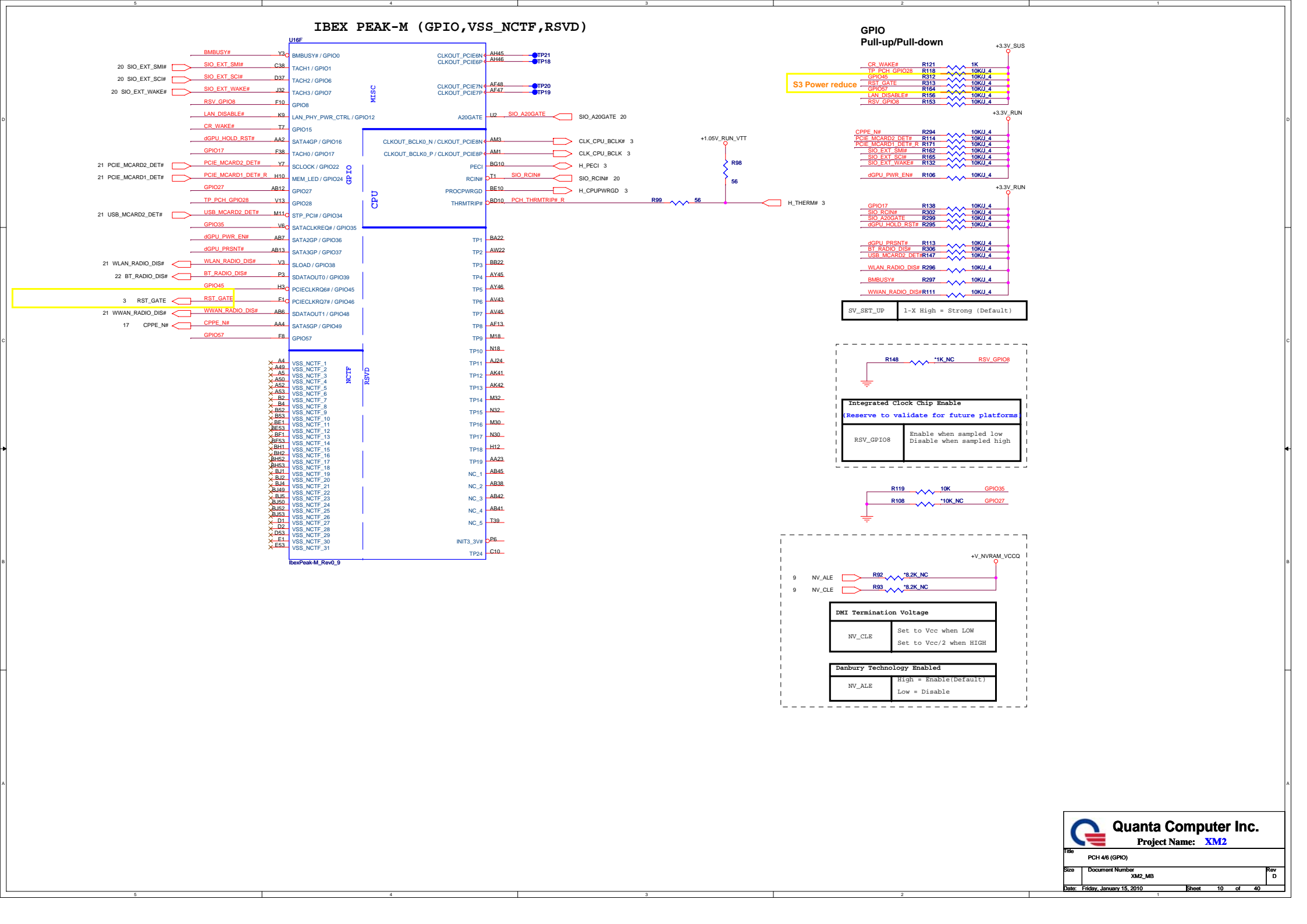
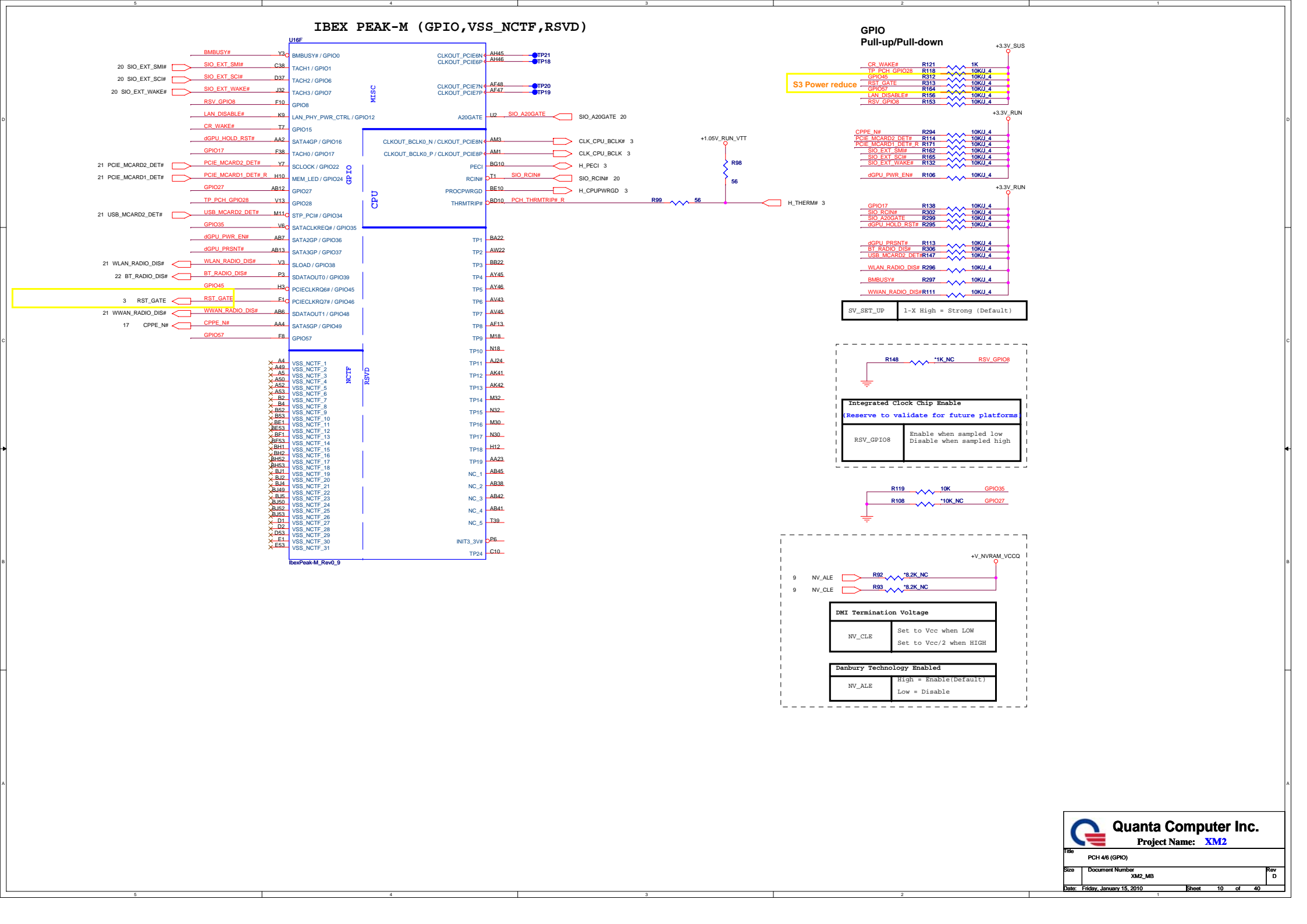
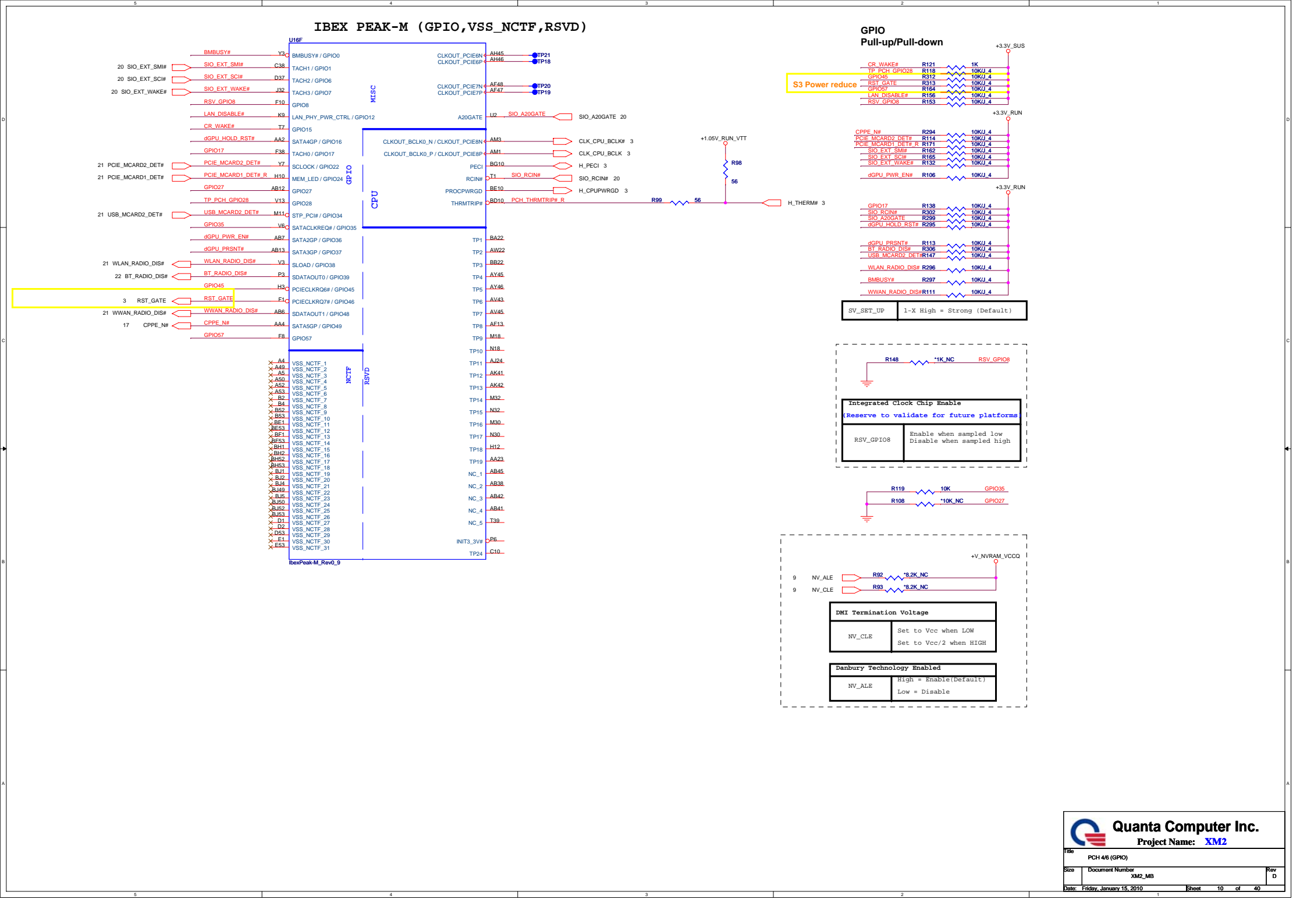
NV_CLE Set to Vcc when LOW
Set to Vcc/2 when HIGH

Danbury Technology Enabled

NV_ALE High = Enable(Default)
Low = Disable

SV_SET_UP 1-X High = Strong (Default)

ibexPeak-M_Rev0_9

[illegible]

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

GPIO Pull-up/Pull-down

S3 Power reduce

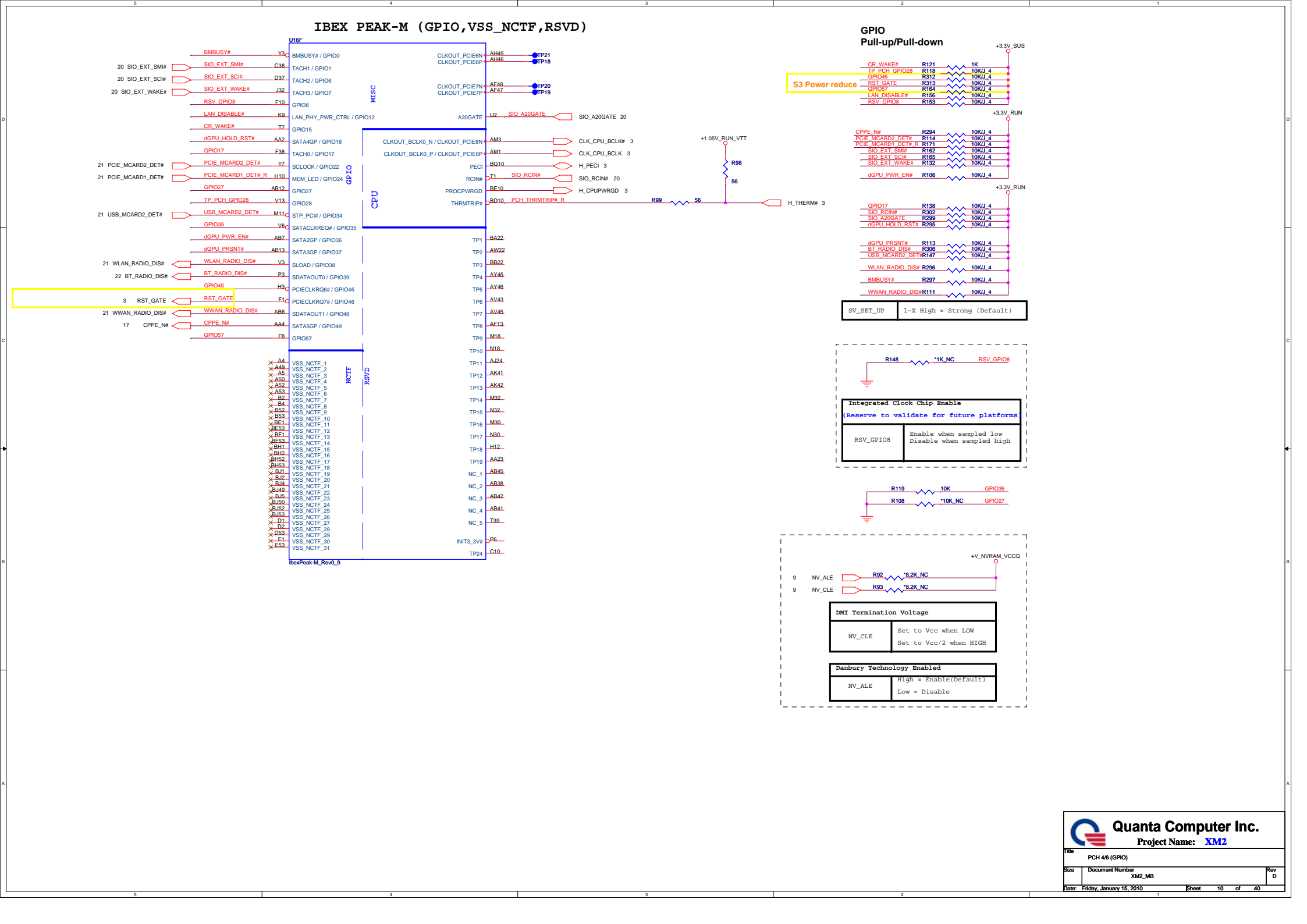
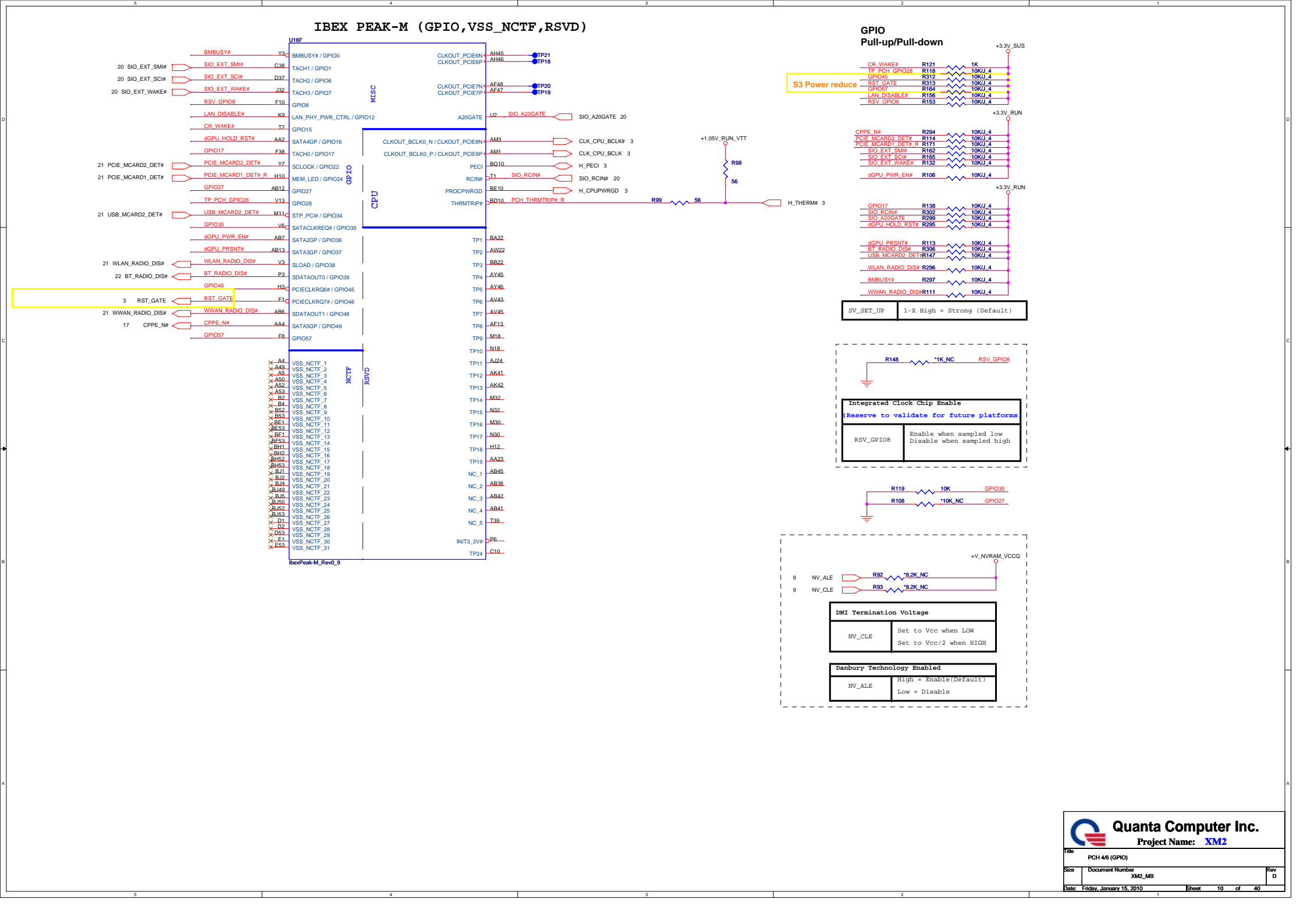
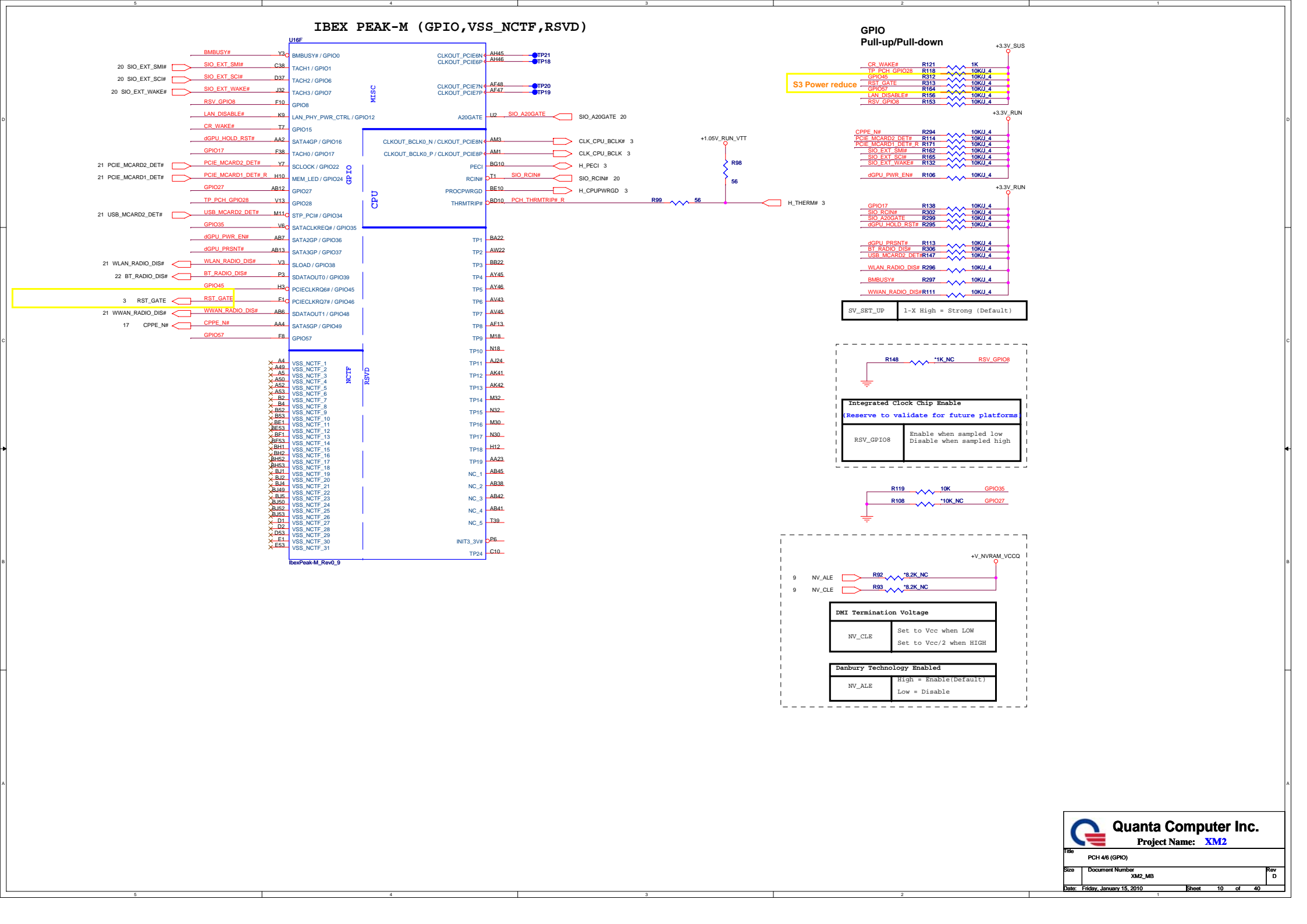
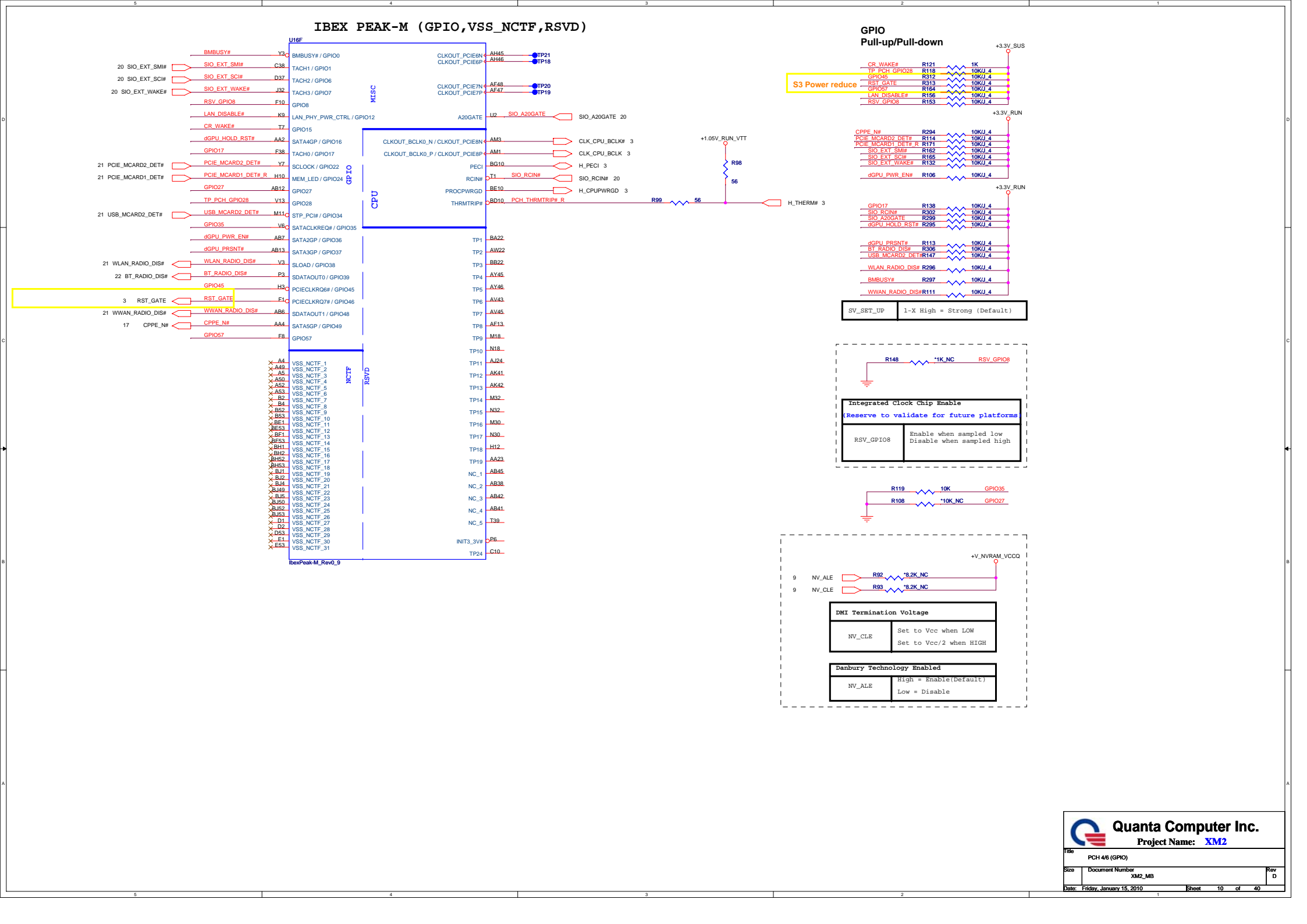
Integrated Clock Chip Enable

DMI Termination Voltage

Danbury Technology Enabled

Quanta Computer Inc.
Project Name: **XM2**

File: PCH 4/6 (GPIO)
Size: Document Number XM2_MB
Date: Friday, January 15, 2010 Sheet 10 of 40

[illegible][illegible][illegible]

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

GPIO Pull-up/Pull-down

S3 Power reduce

Integrated Clock Chip Enable

DMI Termination Voltage

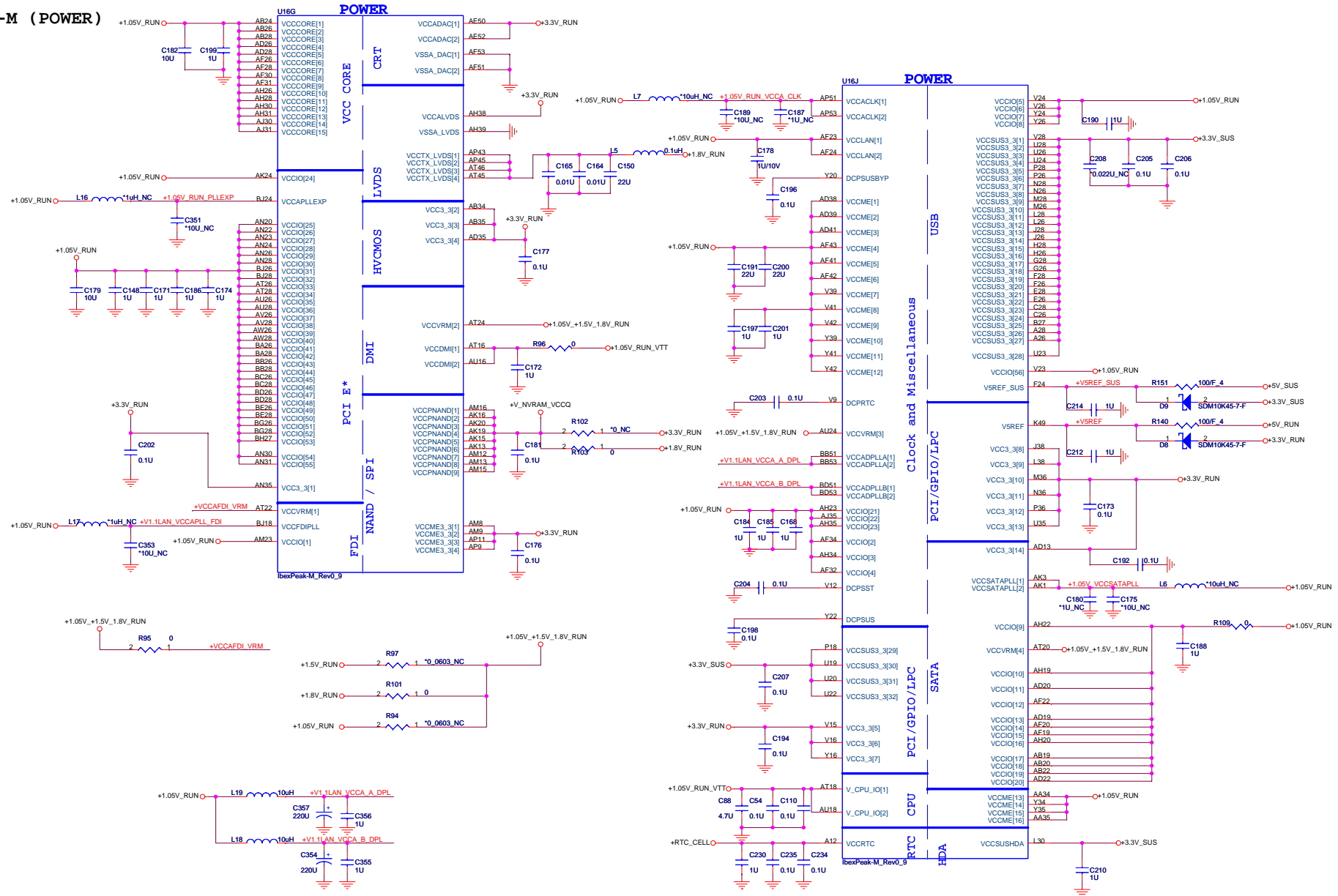
Danbury Technology Enabled

Quanta Computer Inc.
Project Name: **XM2**

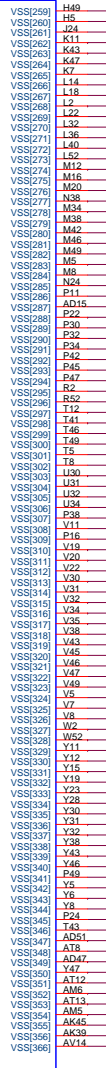
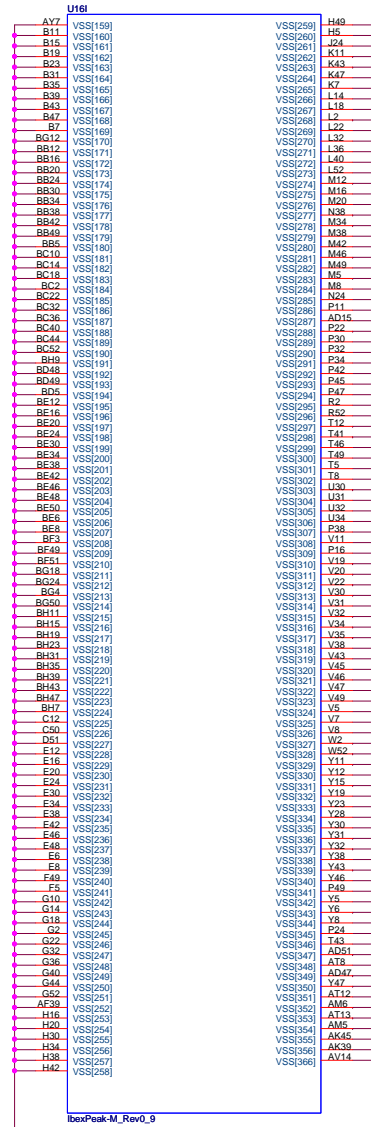
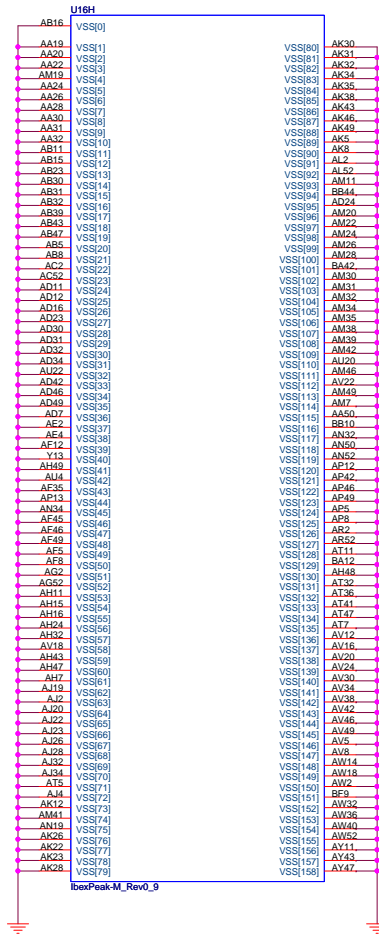
File: PCH 4/6 (GPIO)
Size: Document Number XM2_MB
Date: Friday, January 15, 2010 Sheet 10 of 40

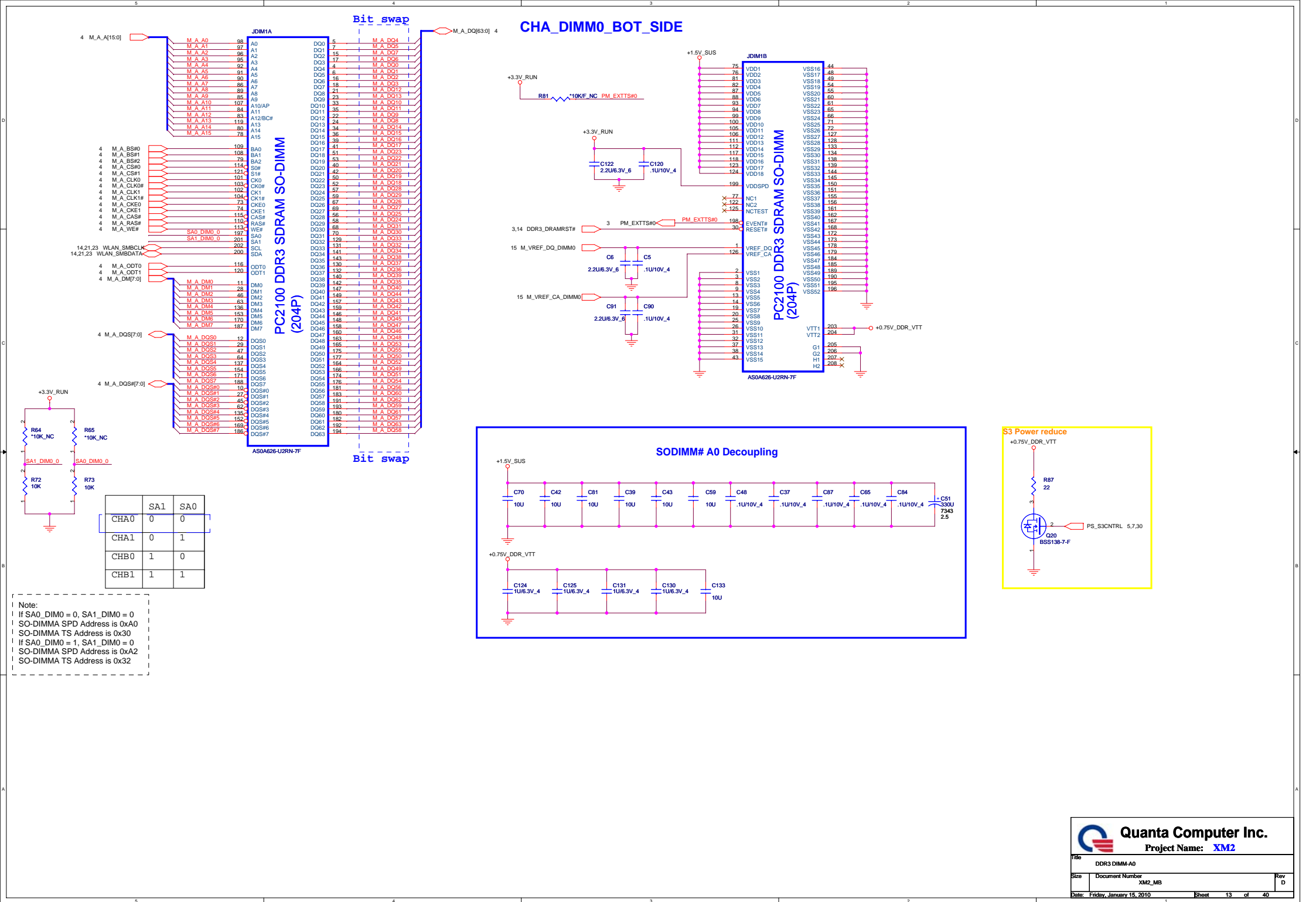
[illegible][illegible]

IBEX PEAK-M (POWER)

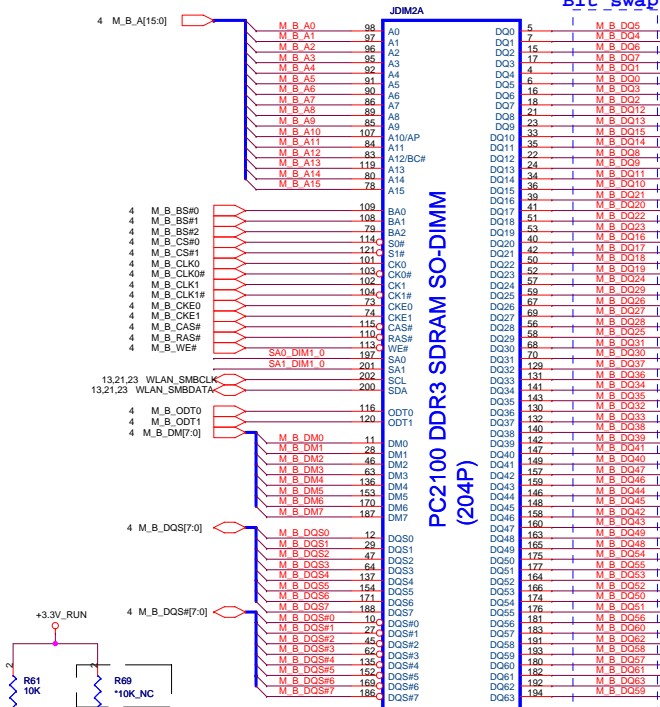


IBEX PEAK-M (GND)

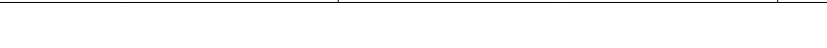
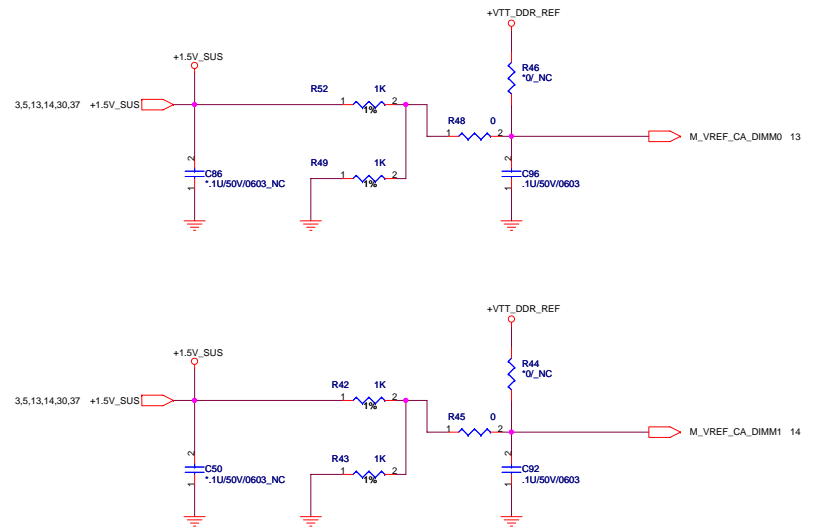
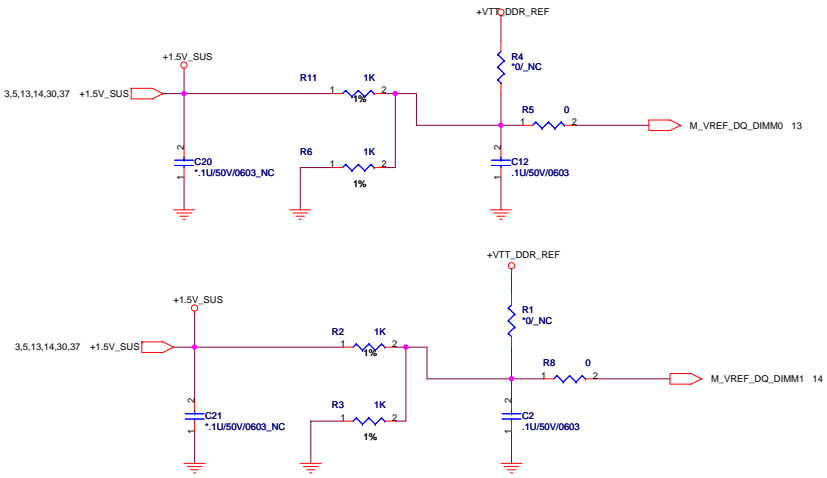


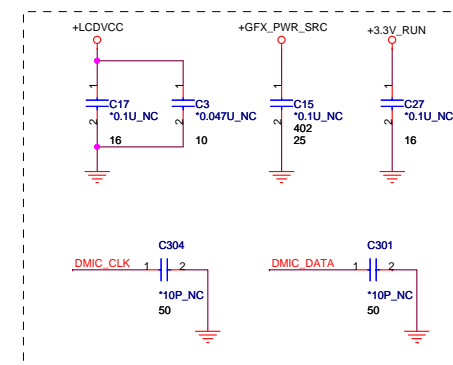
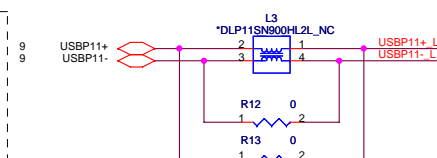
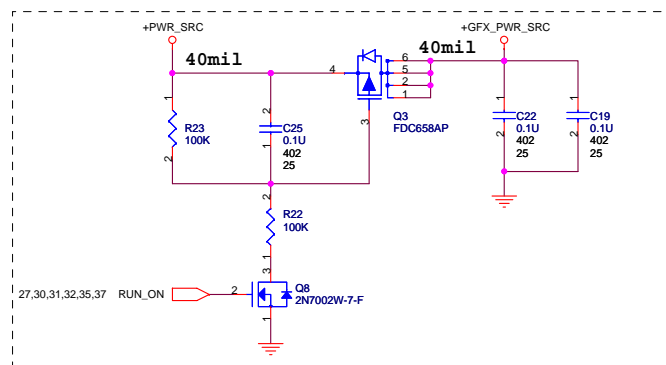
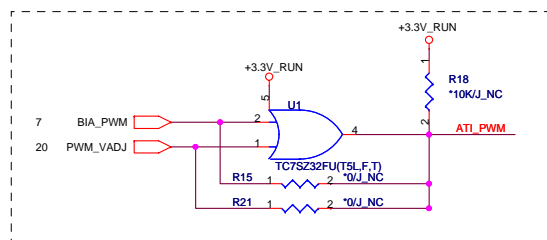
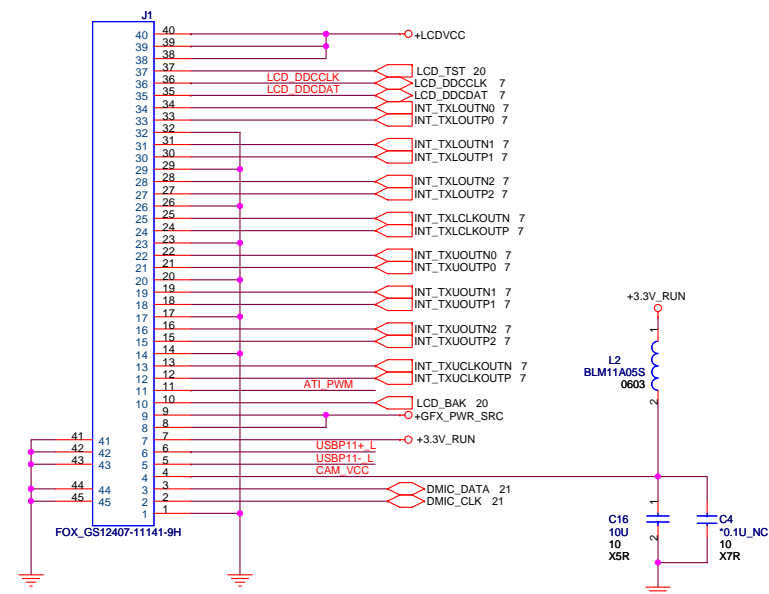
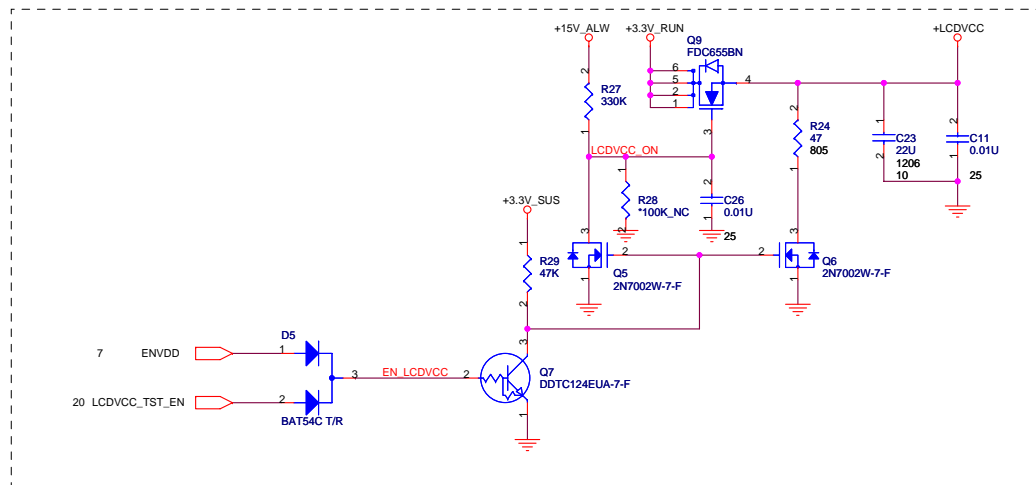


0105CT: Update JDIM4 footprint 5.2mm, STD type.



Fixed SO-DIMM VREF_DQ (M1): Default



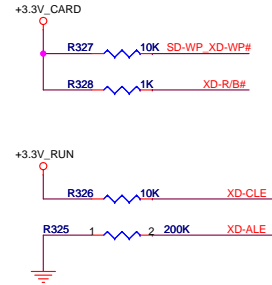
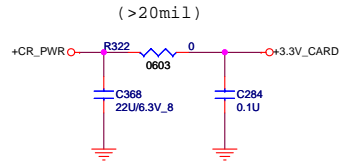
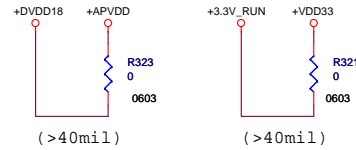


Quanta Computer Inc.
PROJECT : Calpella UMA

Size Document Number
LVDS CONN
Date: Friday, January 15, 2010 Sheet 16 of 40 Rev 1A

Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/XD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1				
CR1_CD2				



MIDO[0..5] Single Skew
Should be smaller +/- 100 mil
for SDA3 Application

3,9,20,21 PLTRST#

9 CLK_PCIE_MINI2#

9 CLK_PCIE_MINI2

+APVDD

+APV18

10uF

0.1uF

1000P

0.1uF

10uF

0.1uF

0.1uF

0.1uF

0.1uF

0.1uF

0.1uF

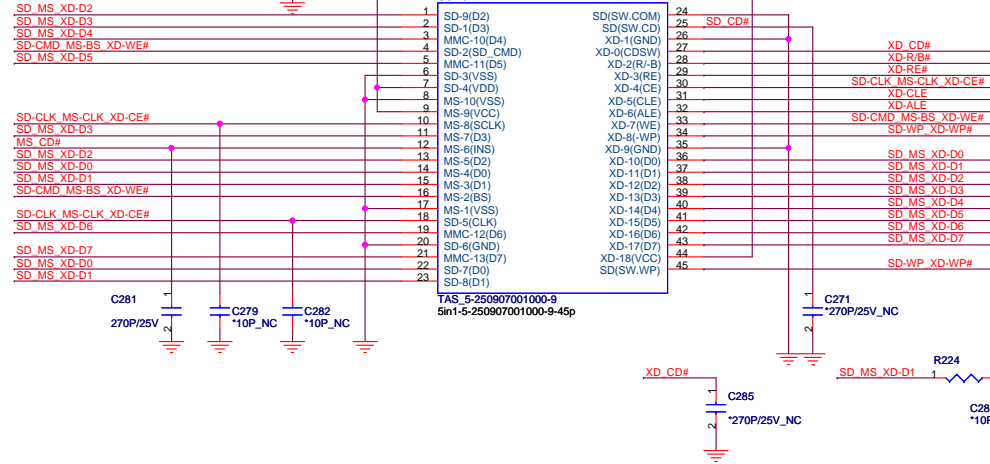
0.1uF

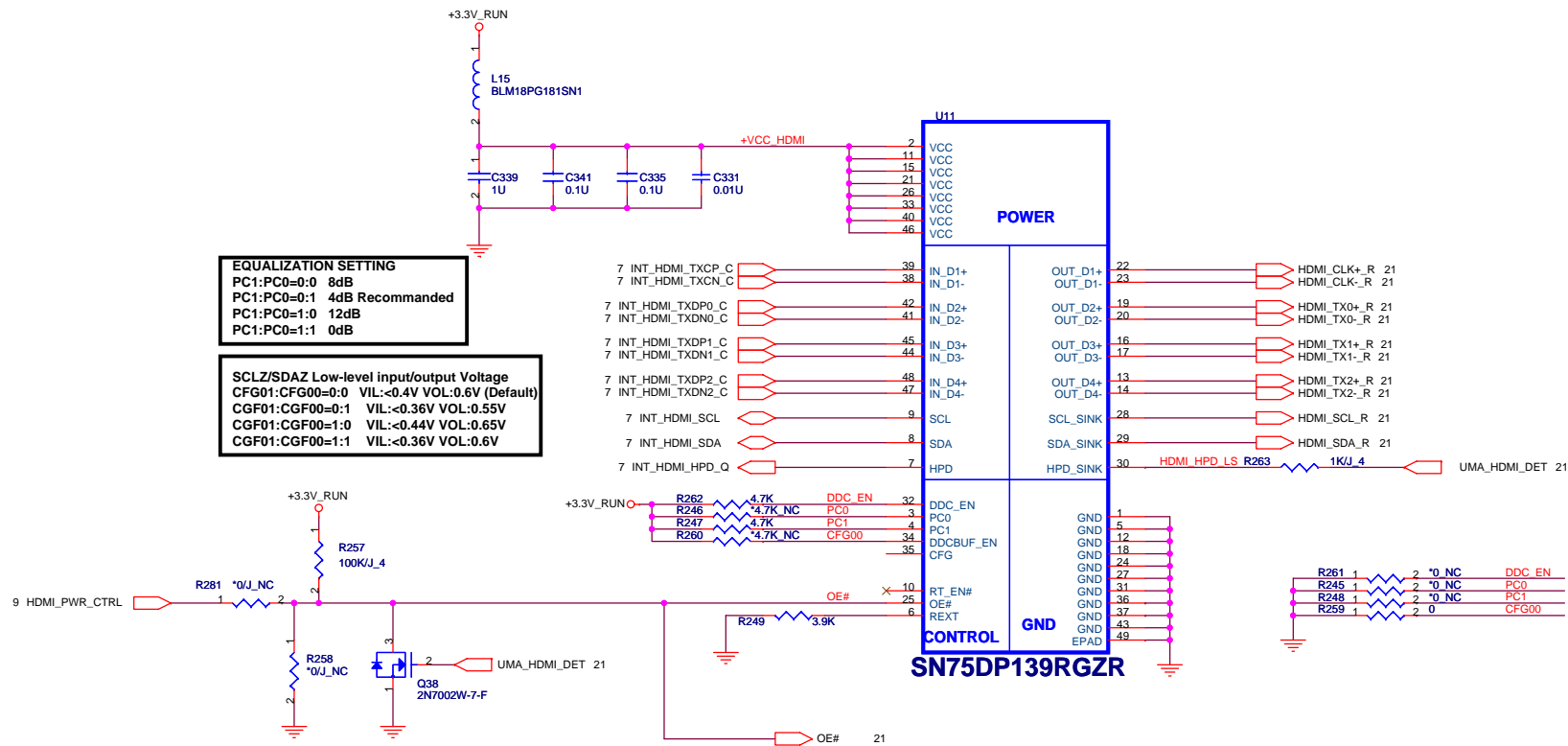
0.1uF

2.2uF cap is no more than
250mils away from the power
pin and a have a min trace
width of 40mils.

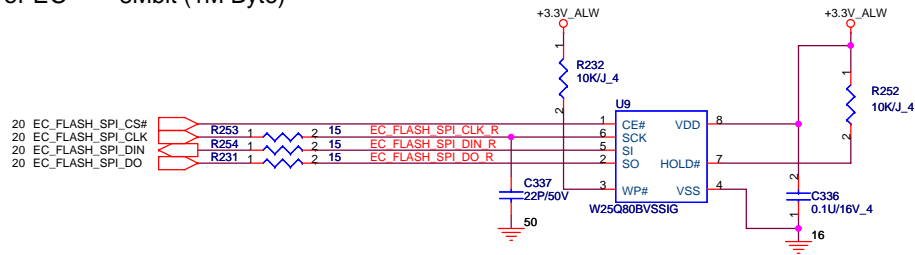
C7577 need close to pin7

C85 need close to pin44

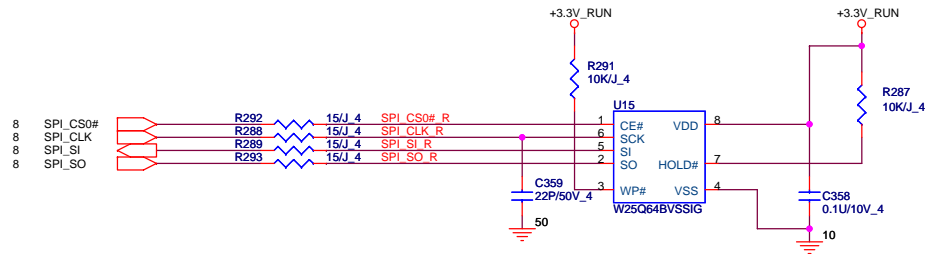




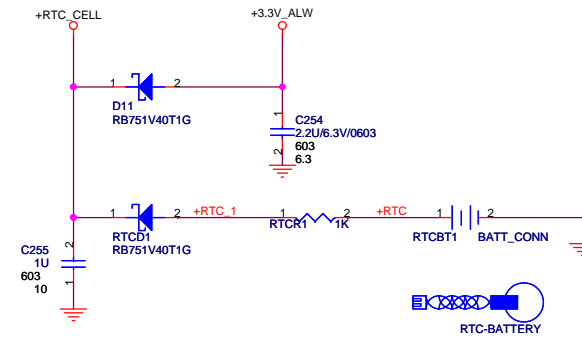
For EC 8Mbit (1M Byte)



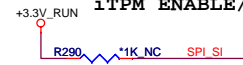
For PCH 64Mbit (8M Byte), SPI



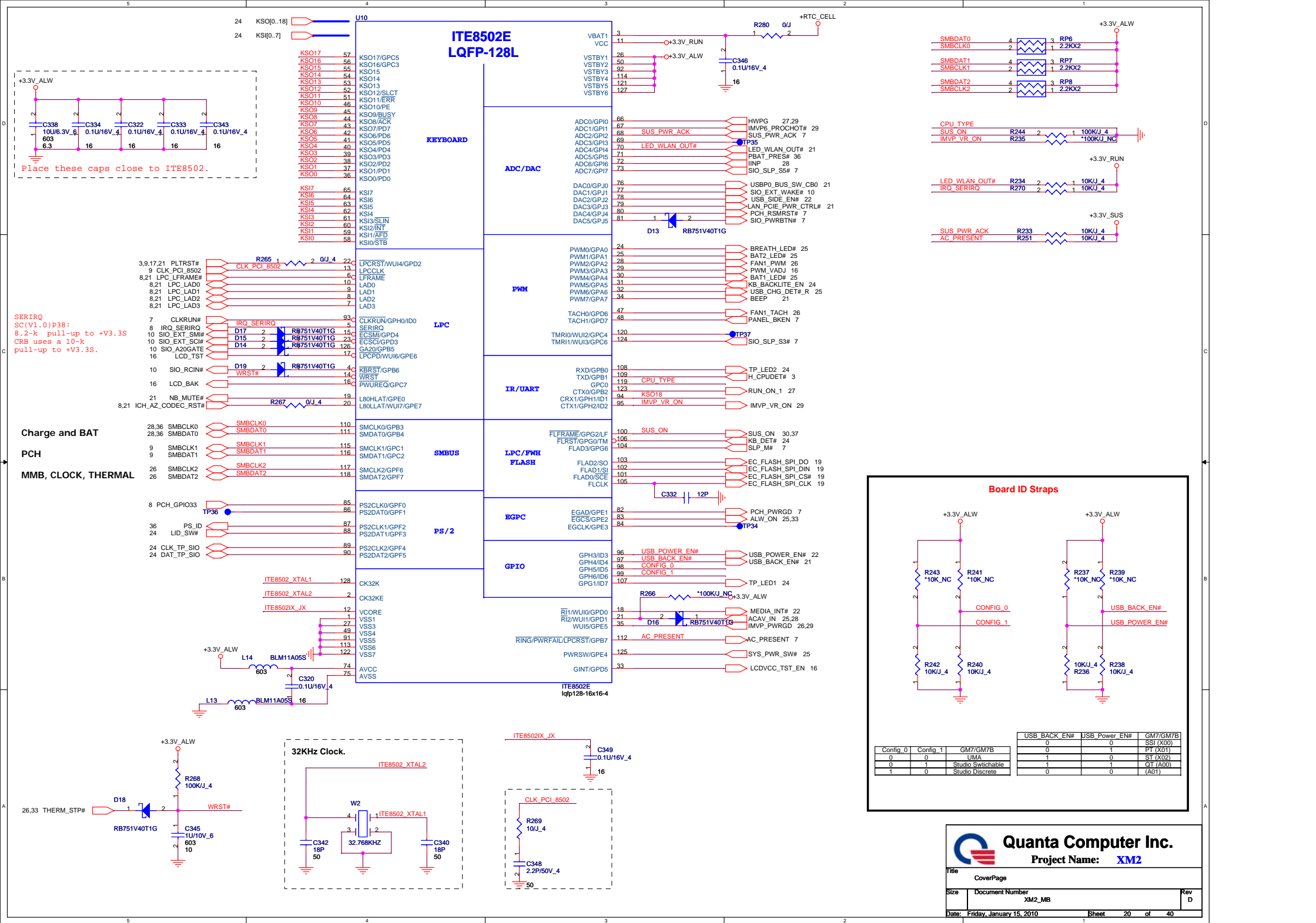
RTC BATTERY

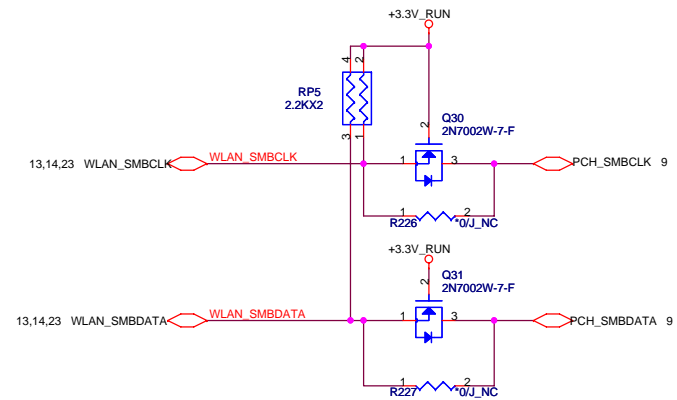
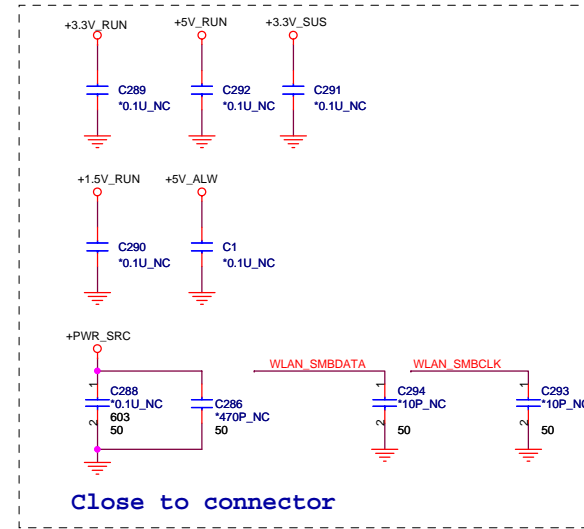
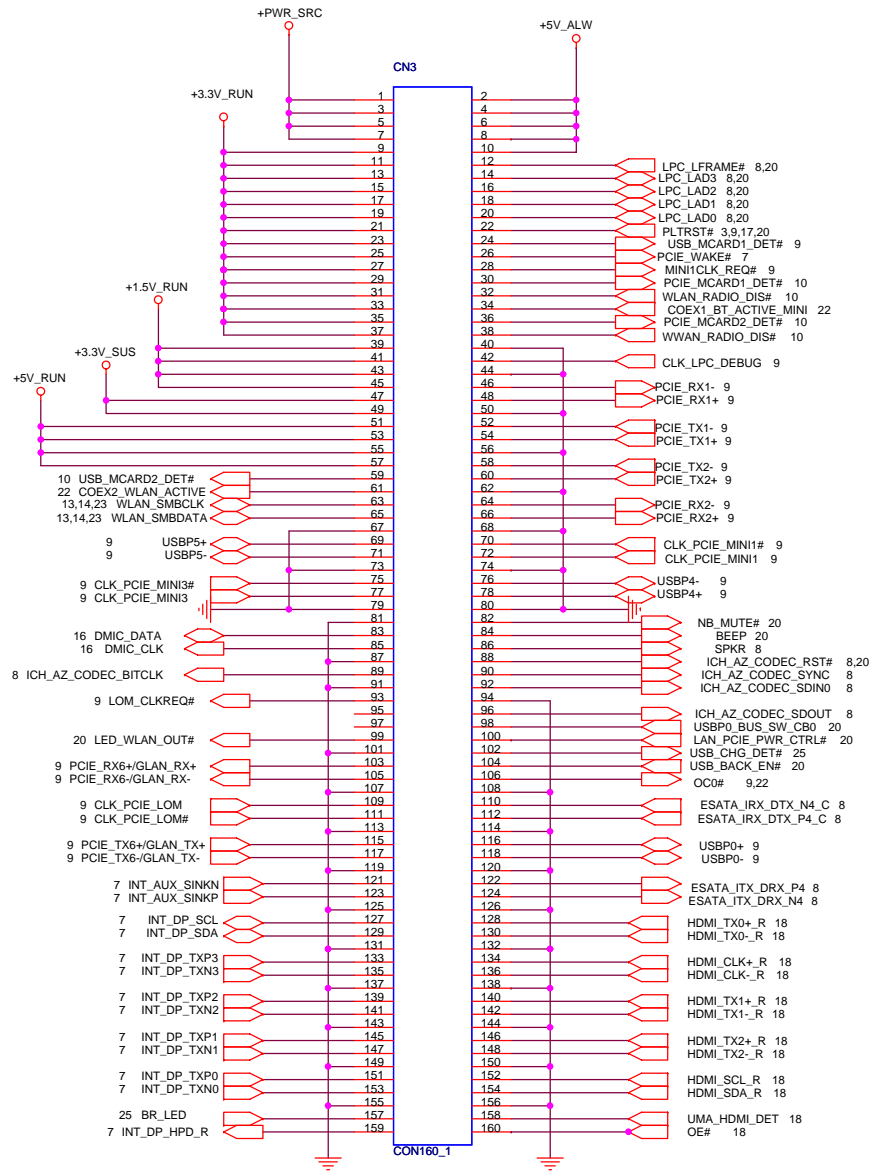


iTPM ENABLE/DISABLE

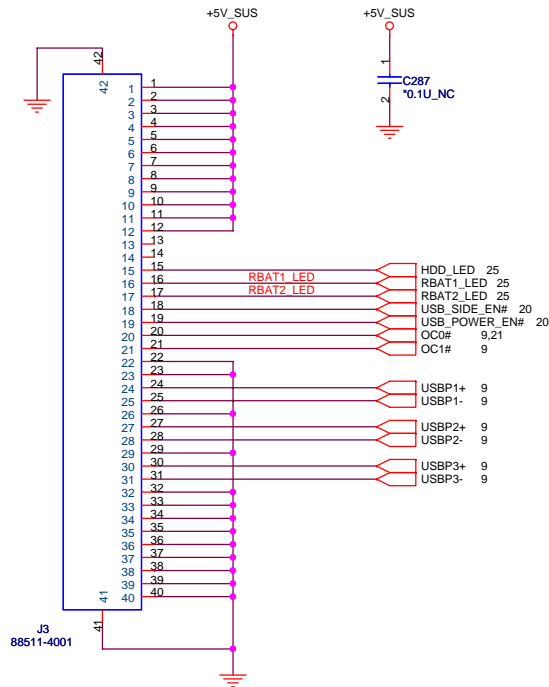


TPM Function	R712
Enable	Mount
Disable	NC (Default)



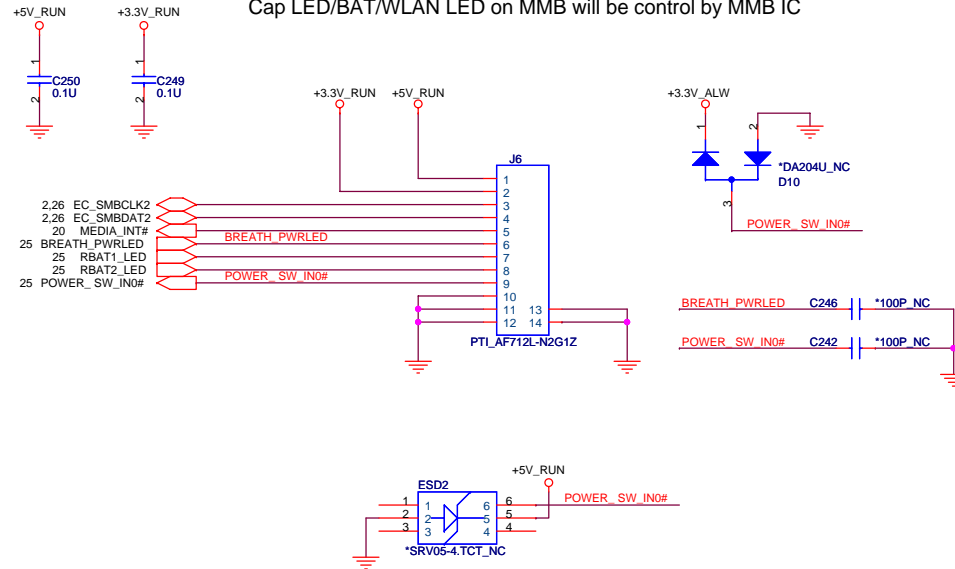


USB IO 40 pins

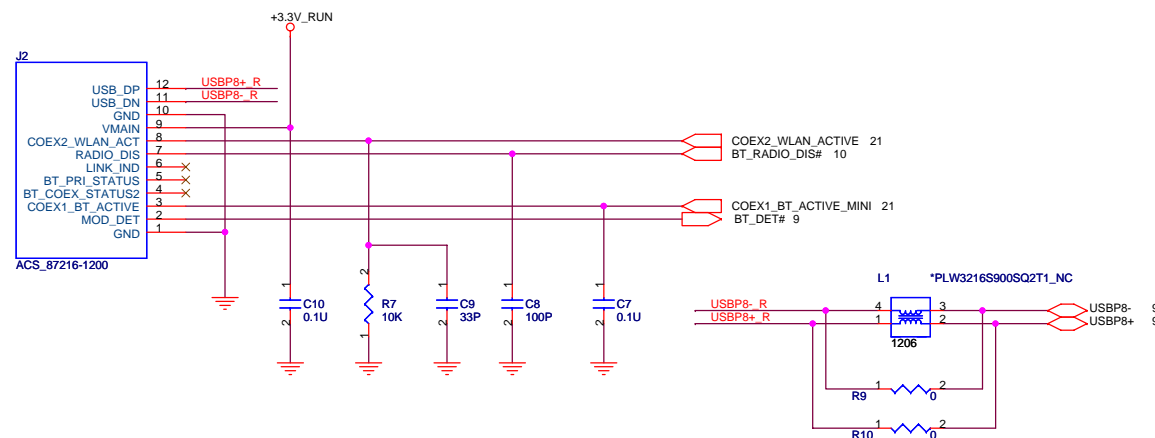


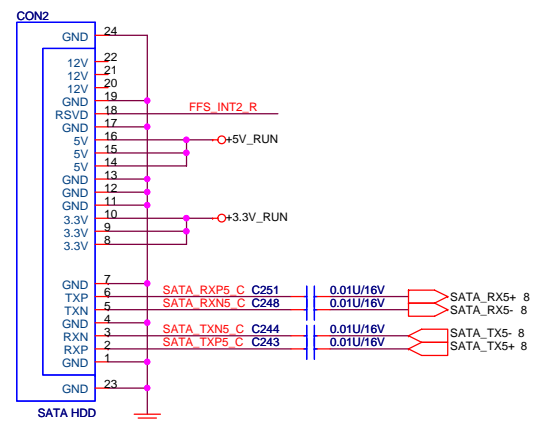
MMB & Power Board 12pins

Cap LED/BAT/WLAN LED on MMB will be control by MMB IC



Support Dell BT3xx series module Bluetooth WTB Conn



[illegible]

DG: Place TX cap close to connector

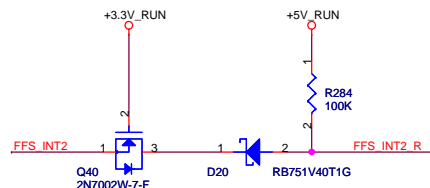
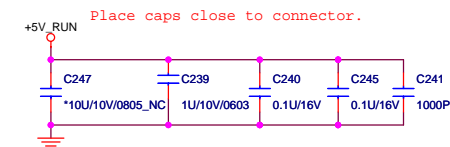
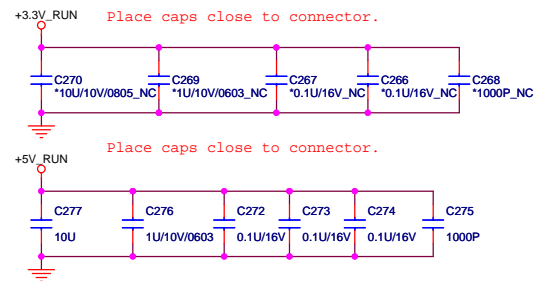
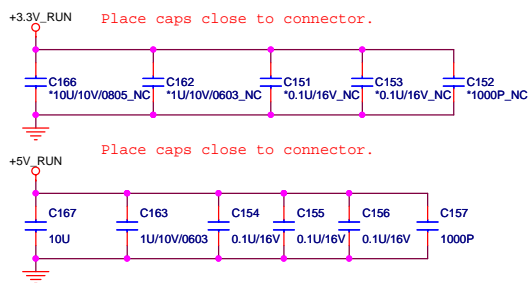
LN27131-C40D-9F

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

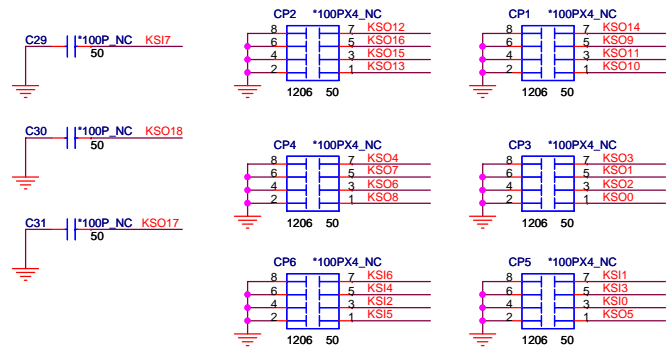
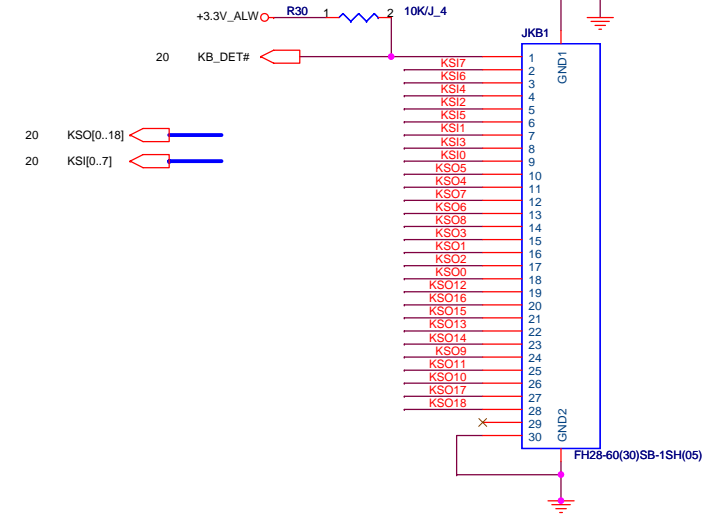
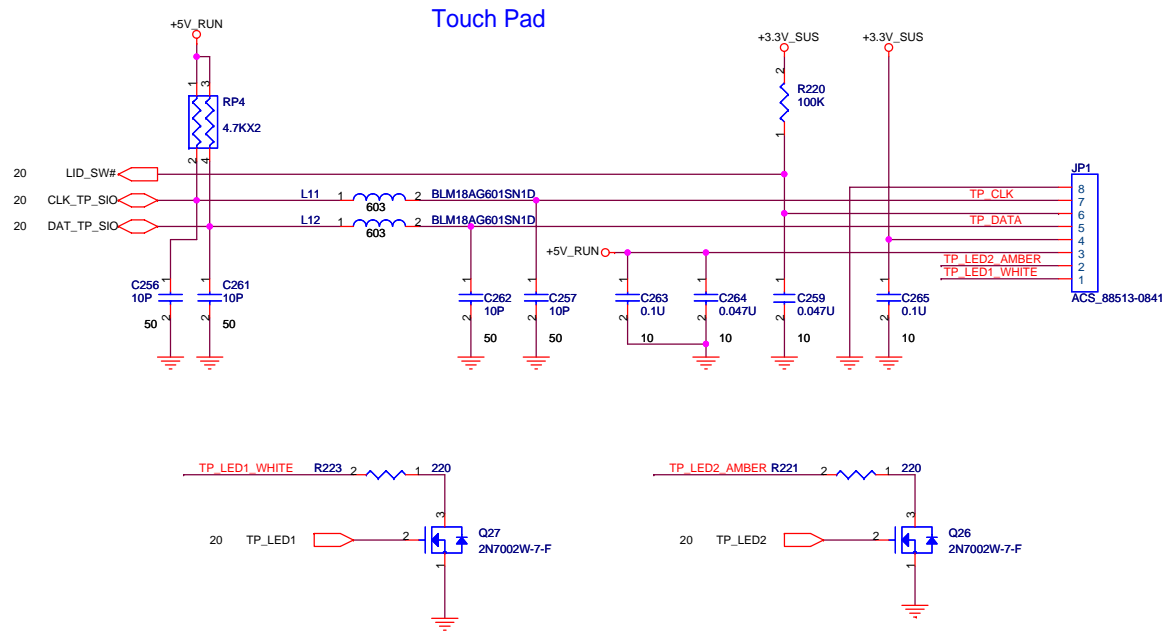
GND1 TXP TXN GND2 RXN RXP GND3 DP +5V +5V MD GND GND

SATA_TXP+ C260 0.01U/16V SATA_TXP- C258 0.01U/16V SATA_RXN+ C253 0.01U/16V SATA_RXN- C252 0.01U/16V

+5V_RUN

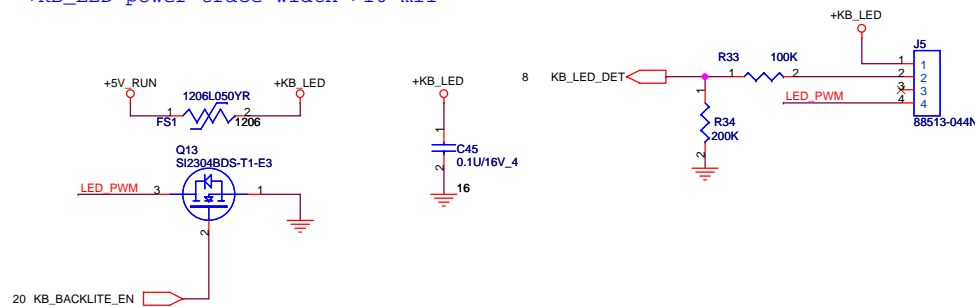


KEYBOARD CONNECTOR



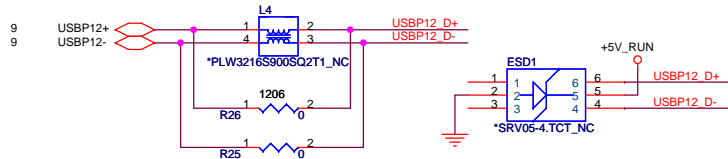
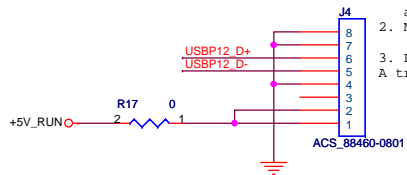
Key board illumination

+KB_LED power trace width >10 mil

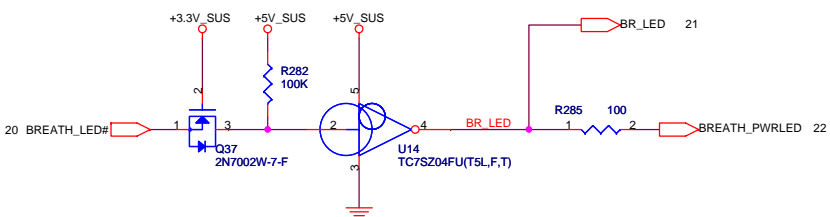
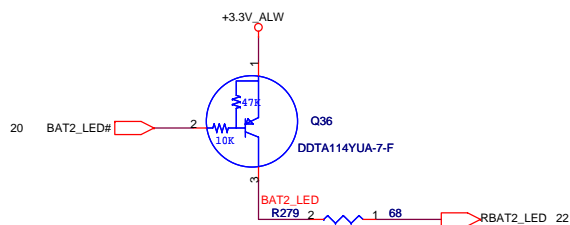
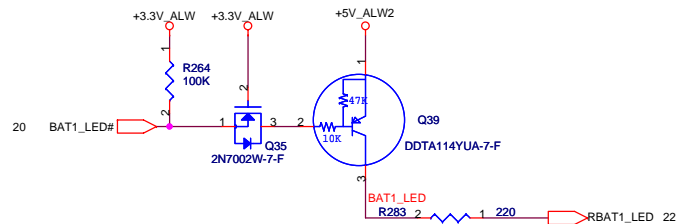


Touch Screen Module

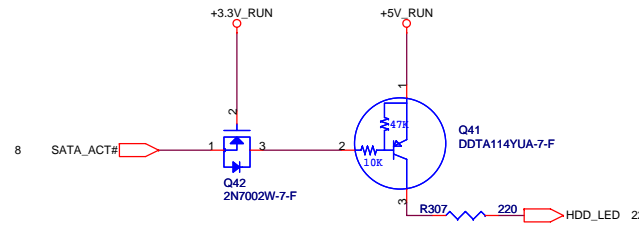
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



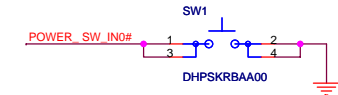
Battery status.



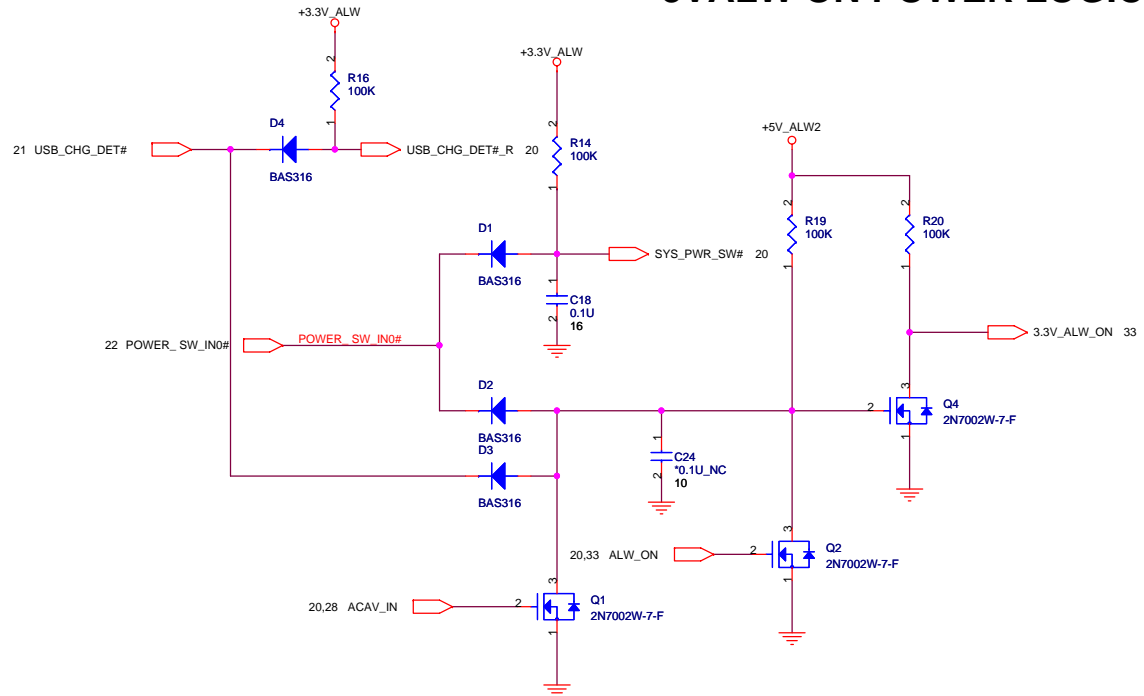
HDD activity LED.

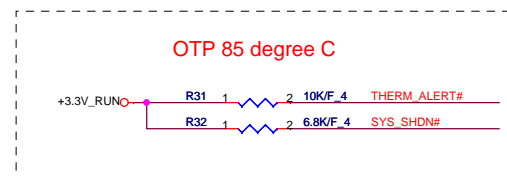
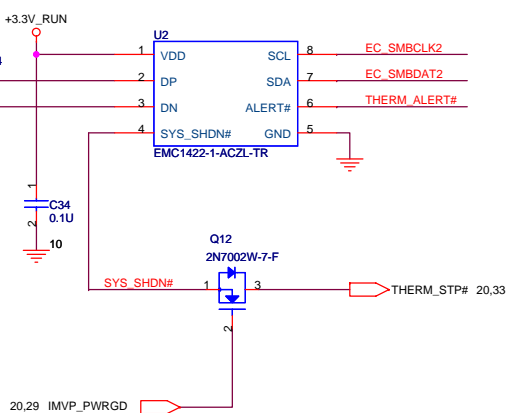
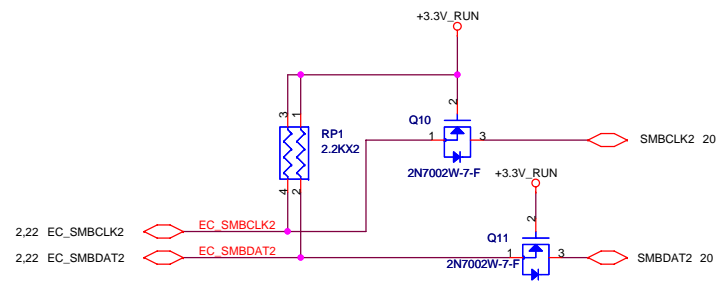
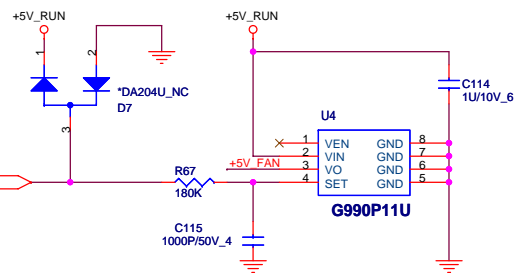
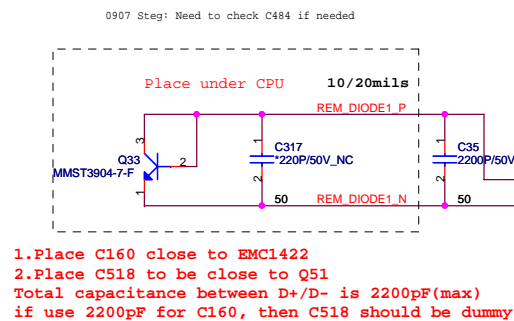
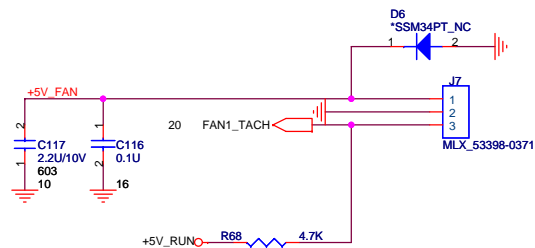


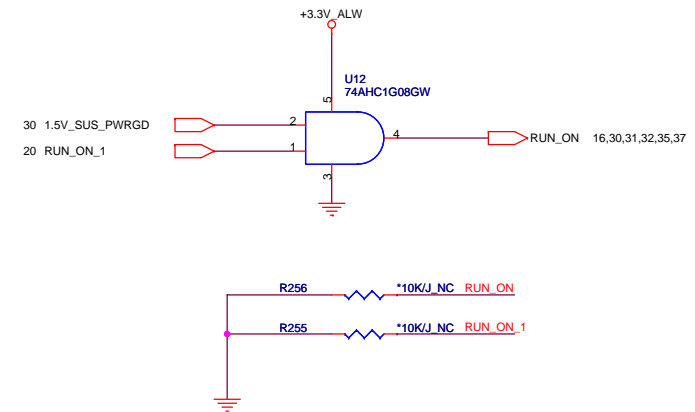
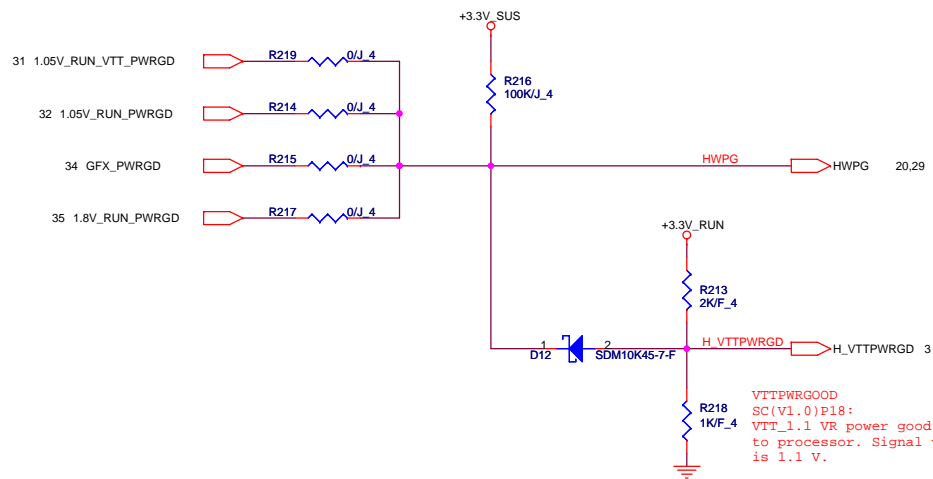
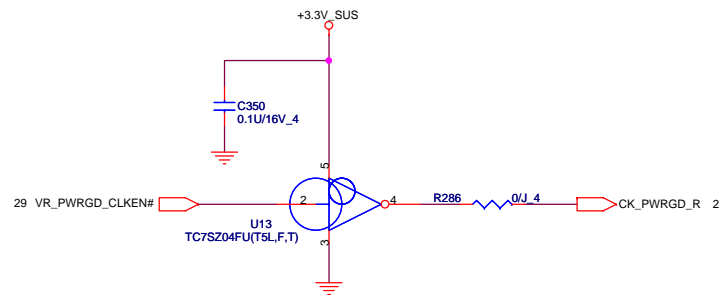
Power button for Engineer

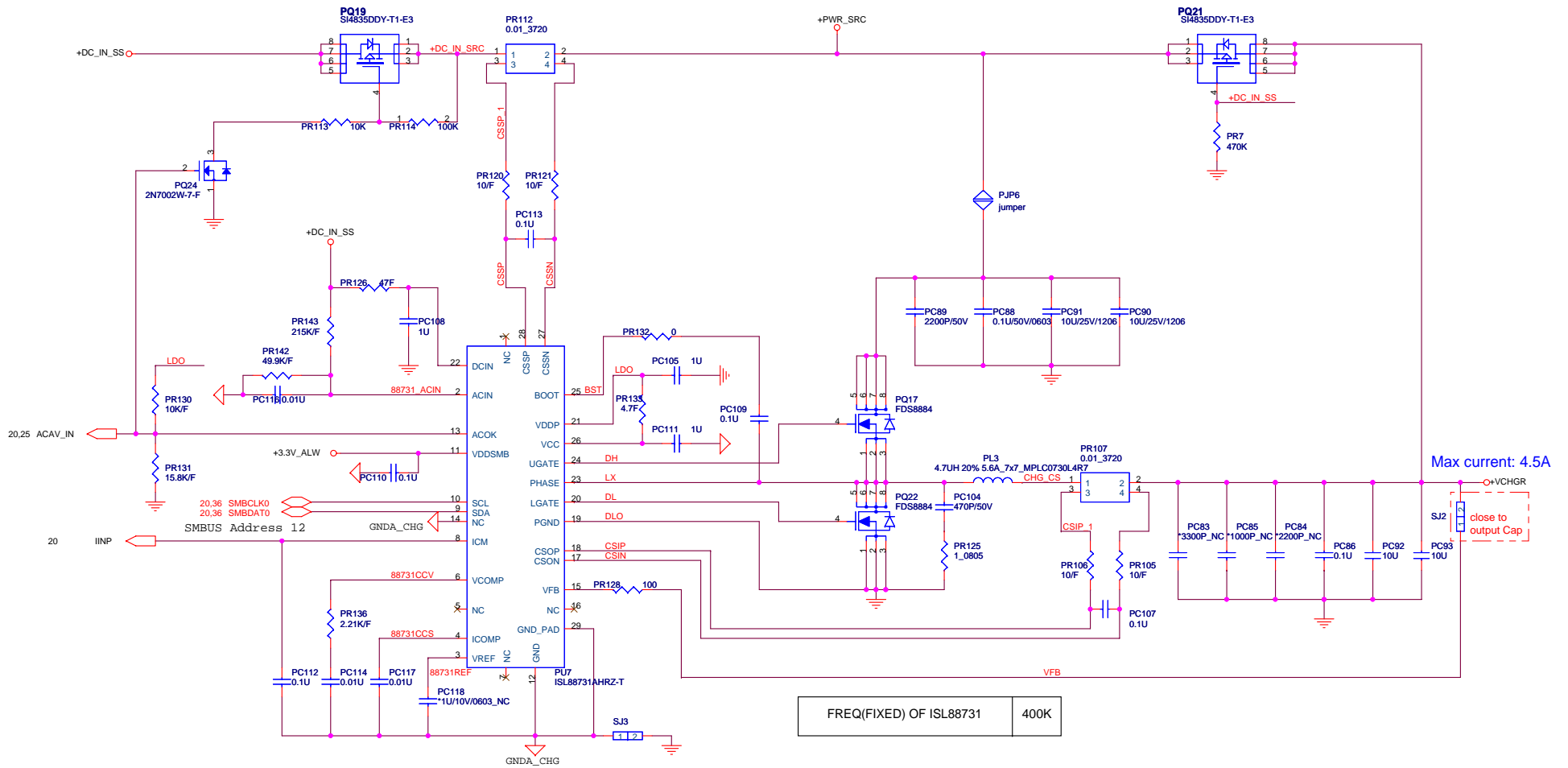


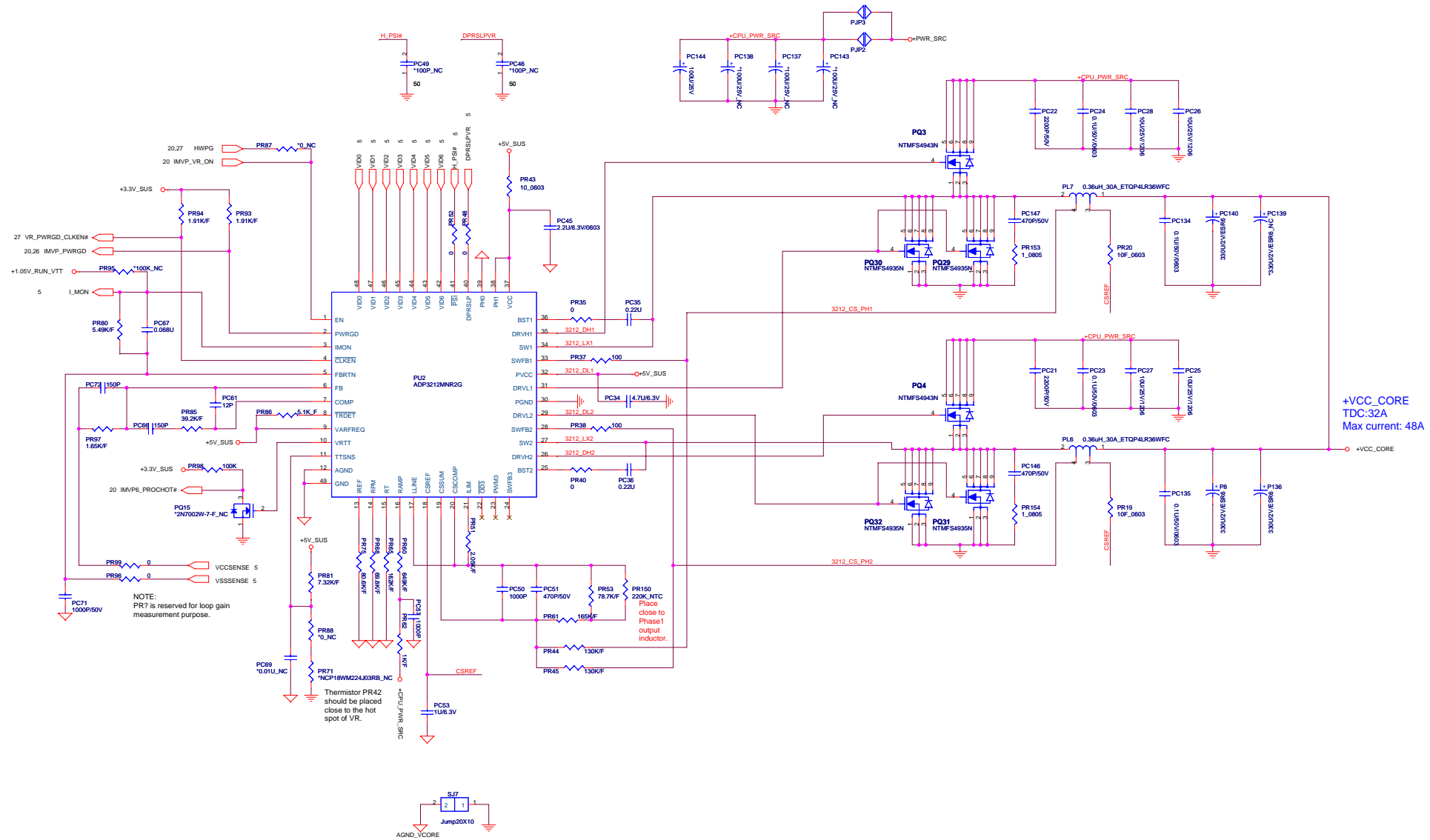
3VALW ON POWER LOGIC



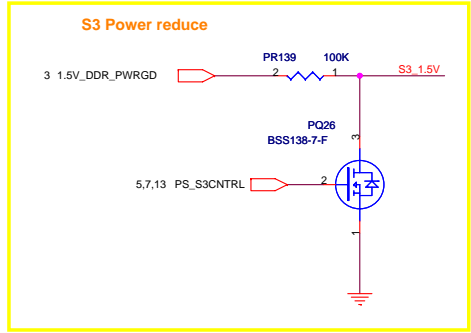








TON	PR67 = 620K
FREQ	400K



VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

VDDQ output voltage selection

FB	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	$0.75V < VDDQ < 3.3V$

Outputs Management by S3, S5 control

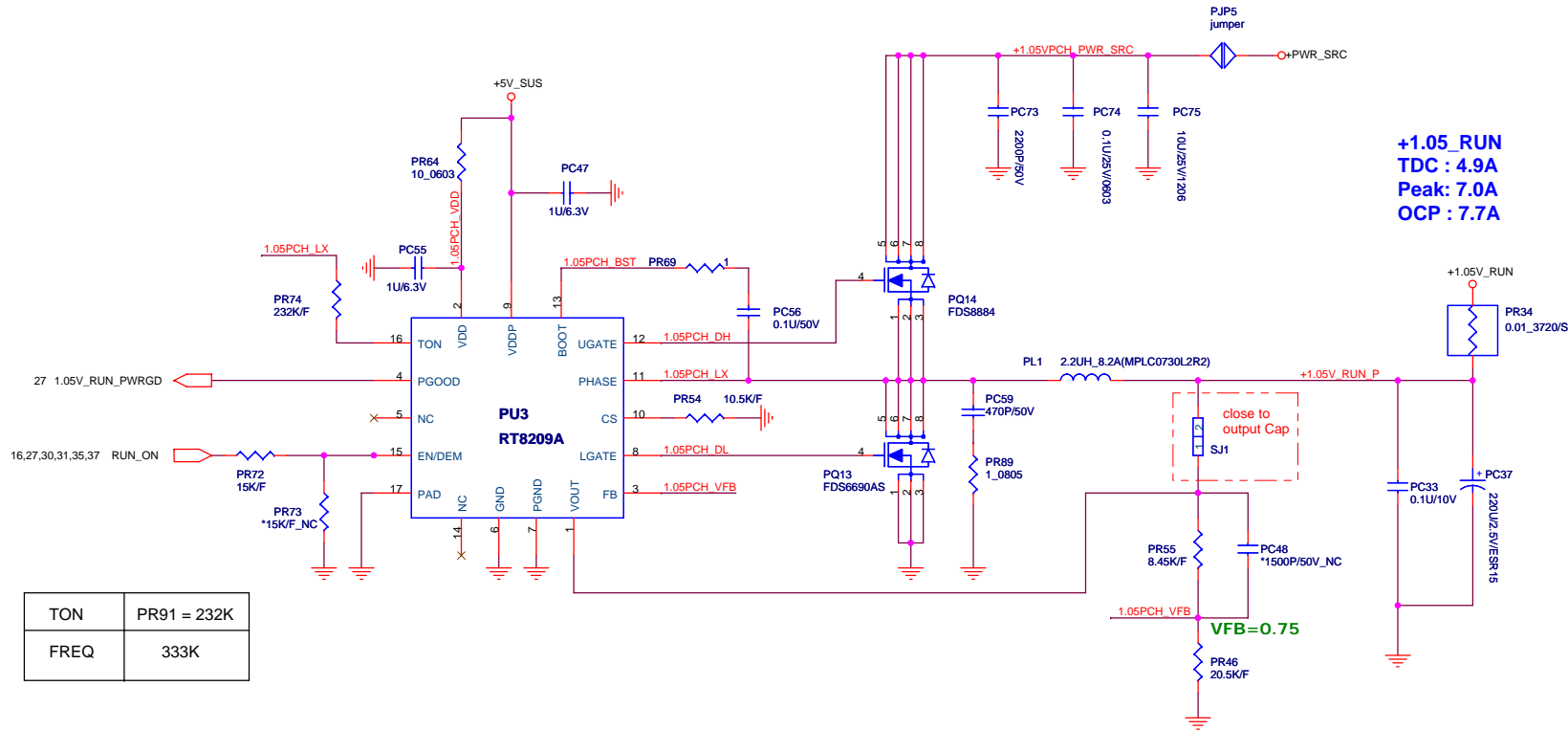
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

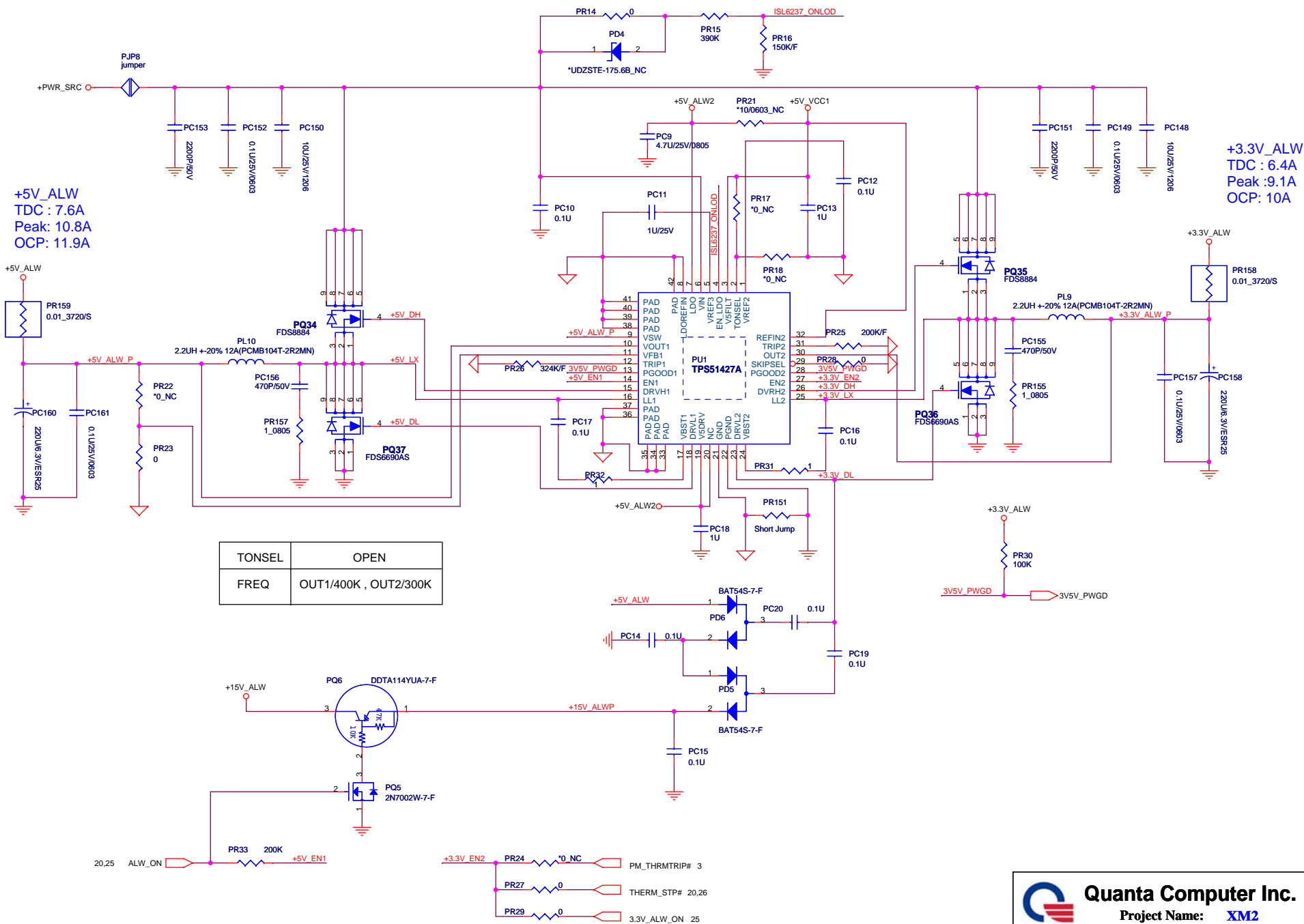


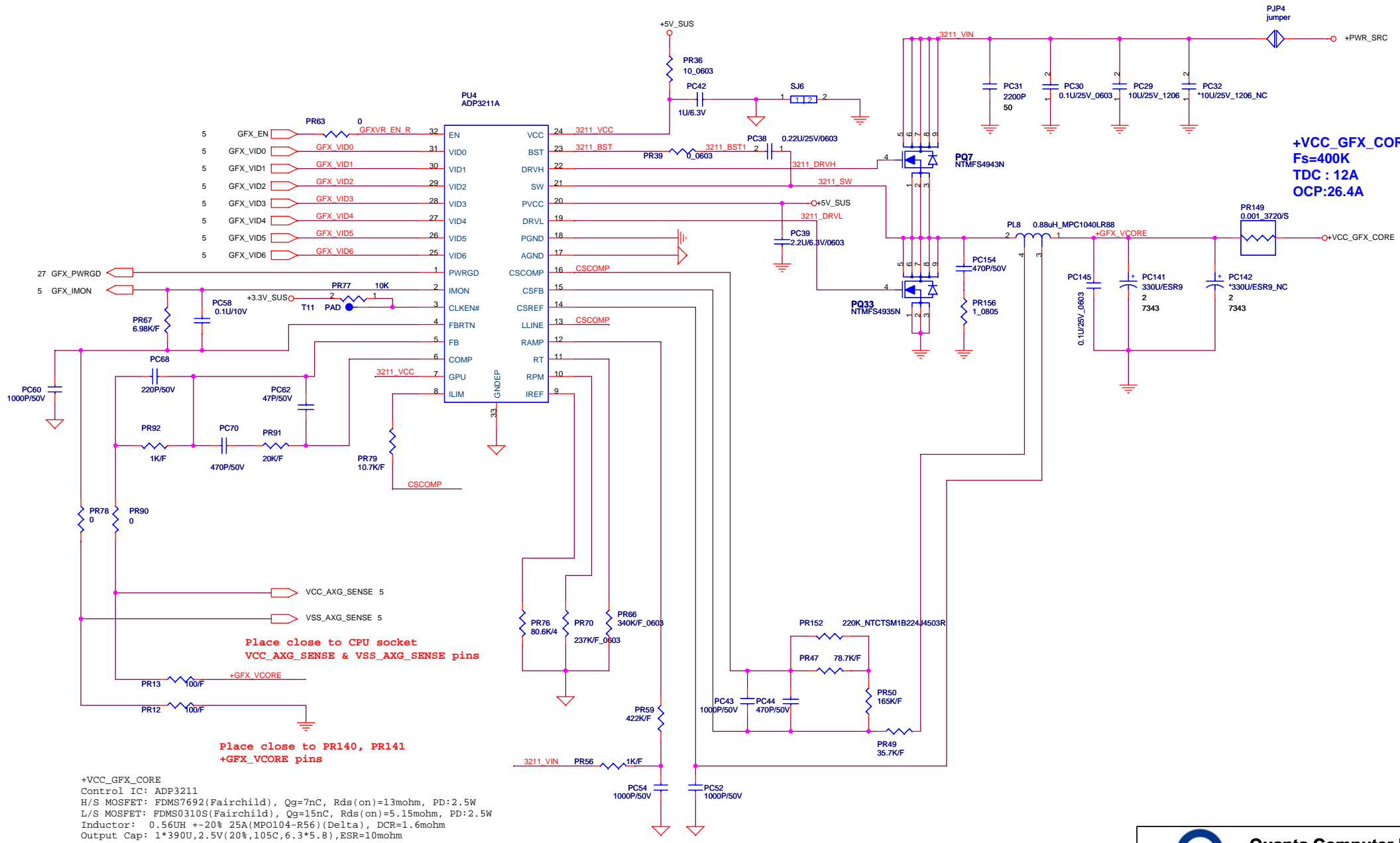
Quanta Computer Inc.

Project Name: **XM2**

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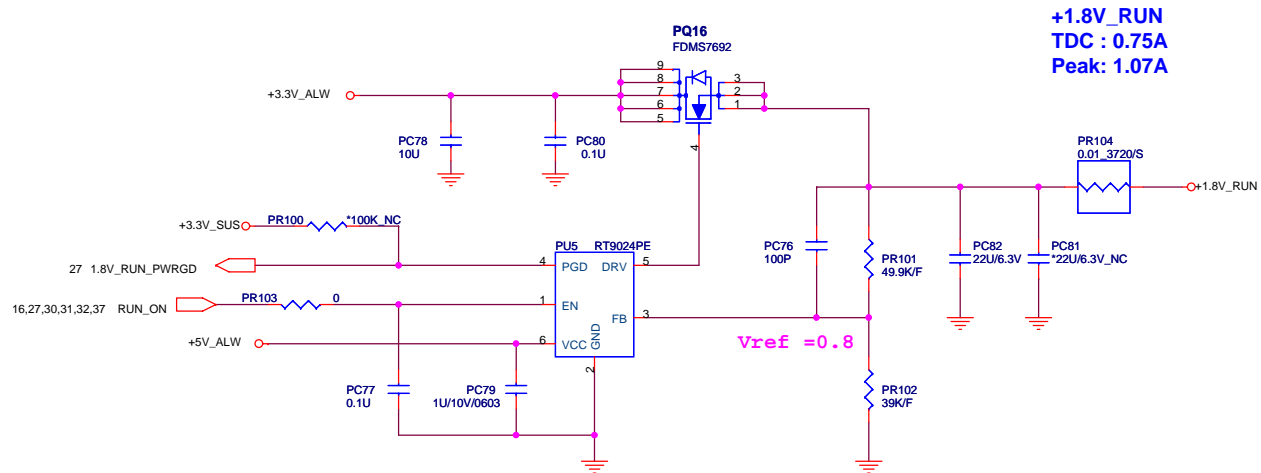


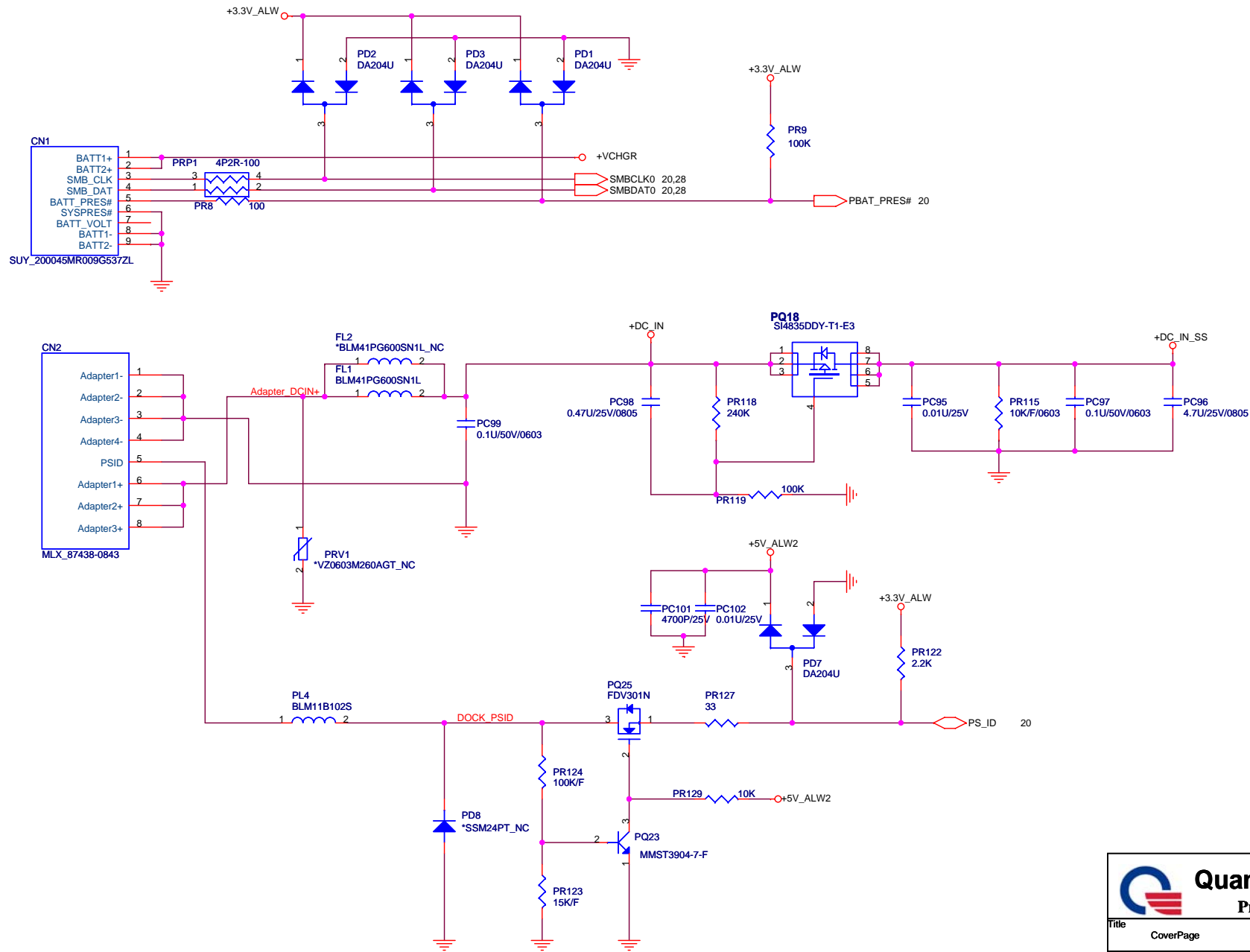
+VCC_GFX_CORE
Fs=400K
TDC : 12A
OCP:26.4A

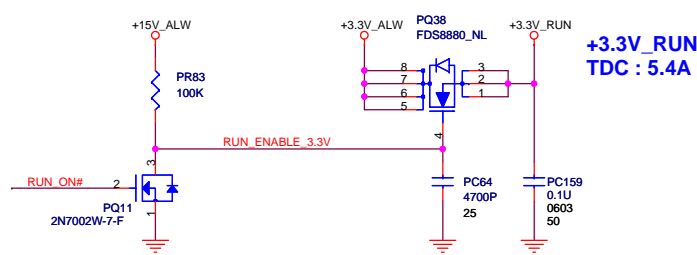
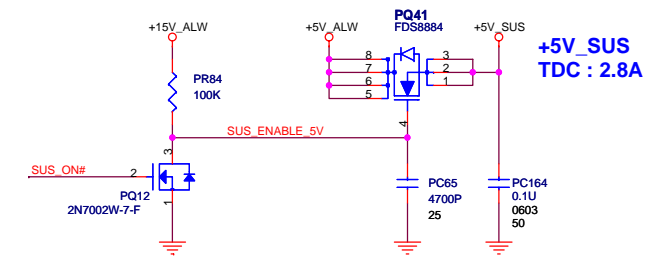
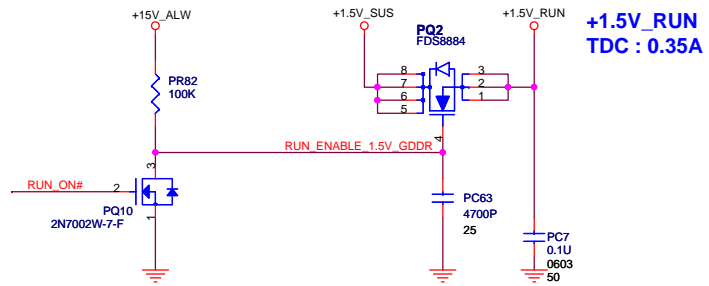
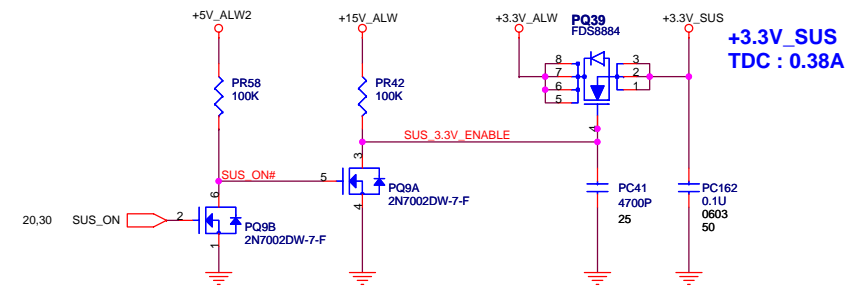
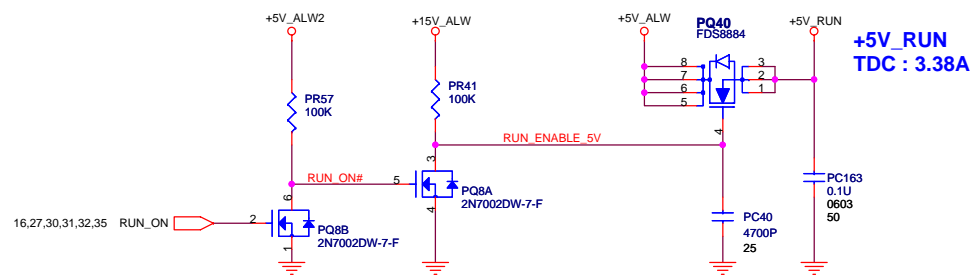
Place close to CPU socket
VCC_AXG_SENSE & VSS_AXG_SENSE pins

Place close to PR140, PR141
+GFX_VCORE pins

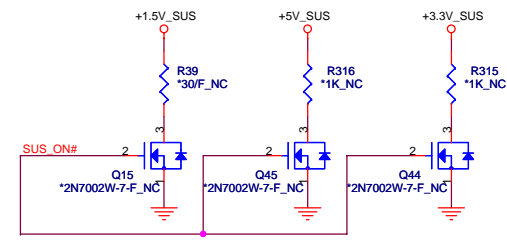
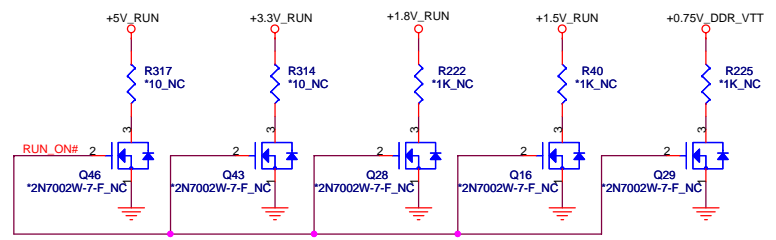
+VCC_GFX_CORE
Control IC: ADP3211
H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
Inductor: 0.56UH +-20% 25A(MP0104-R56)(Delta), DCR=1.6mohm
Output Cap: 1*390U, 2.5V(20%, 105C, 6.3*5.8), ESR=10mohm








Reserve discharge path



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